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# Fig. 1

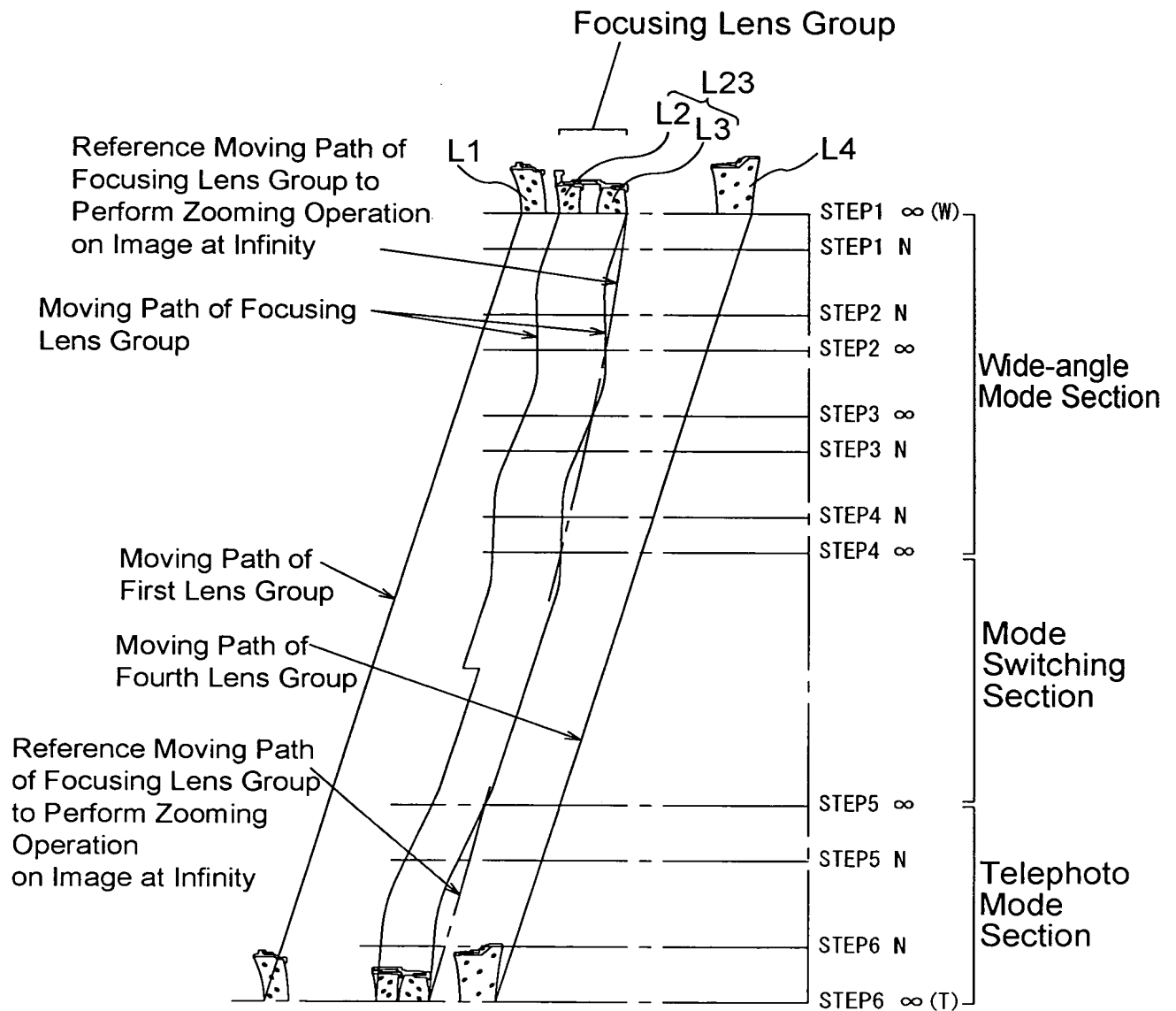
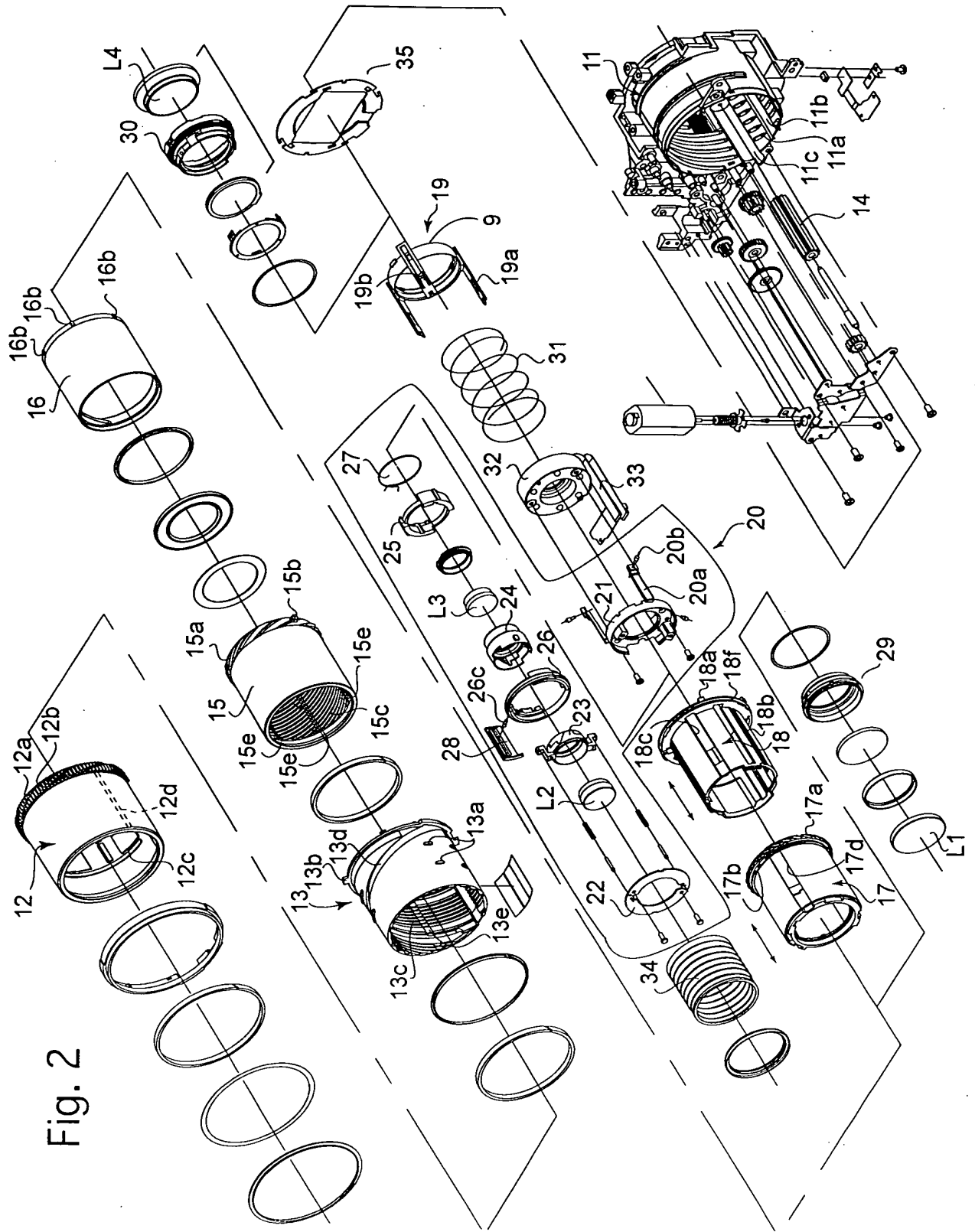


Fig. 2



**Fig. 3**

Fig. 3 is a cross-sectional view of a semiconductor device. The device includes a substrate (10) and a gate stack (11, 12, 13, 14, 15, 15c, 15d(15d2)). A channel region (16) is formed in the substrate, and a source/drain region (17) is formed in the substrate. A contact layer (18) is formed on the gate stack, and a passivation layer (19) is formed on the contact layer. A metal layer (20) is formed on the passivation layer. Various other layers and structures are labeled with numbers 1 through 35. The device is shown in a cross-section along a dashed line L1-L4, with a vertical dashed line L23(20) indicating a specific plane of interest.

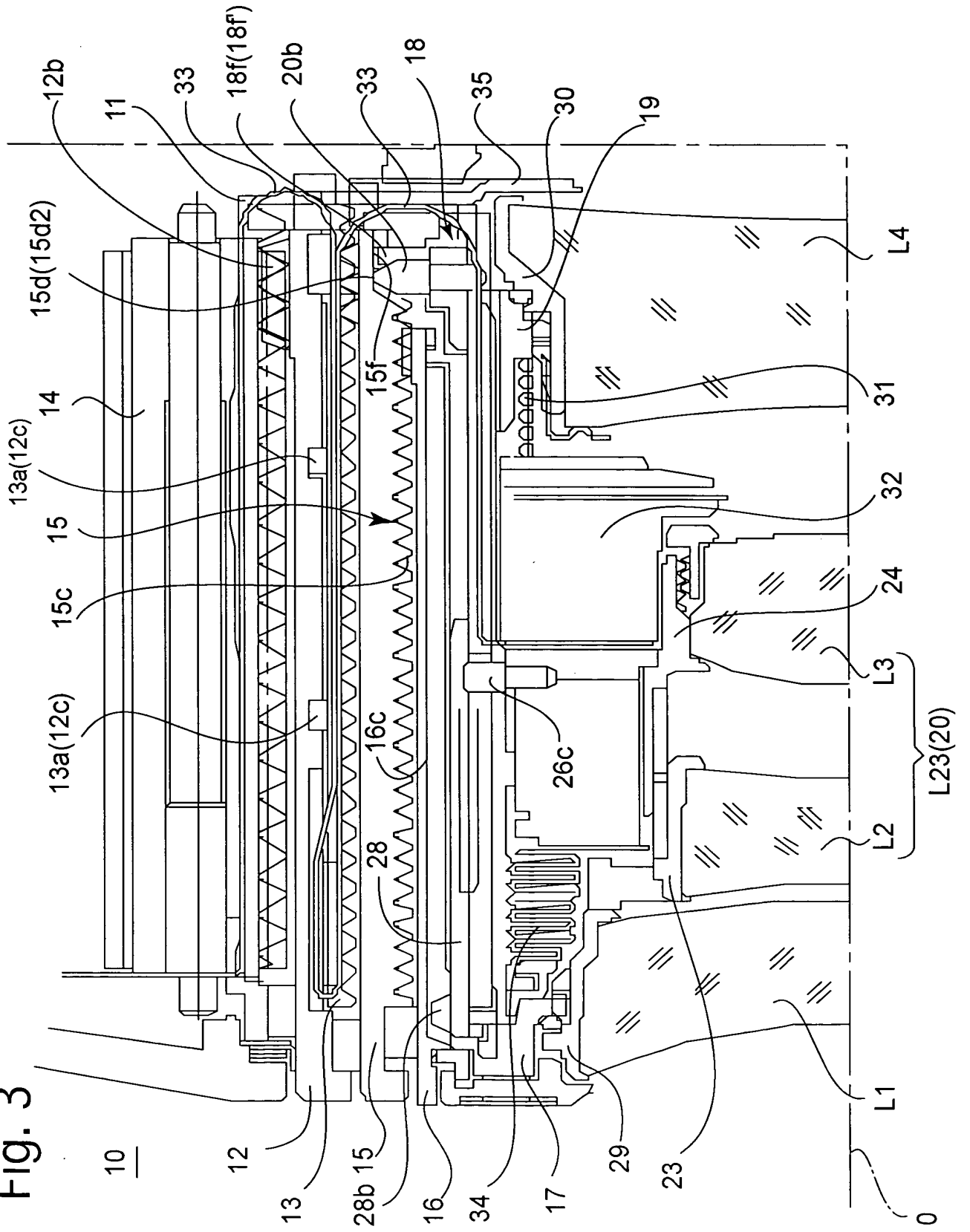


Fig. 4

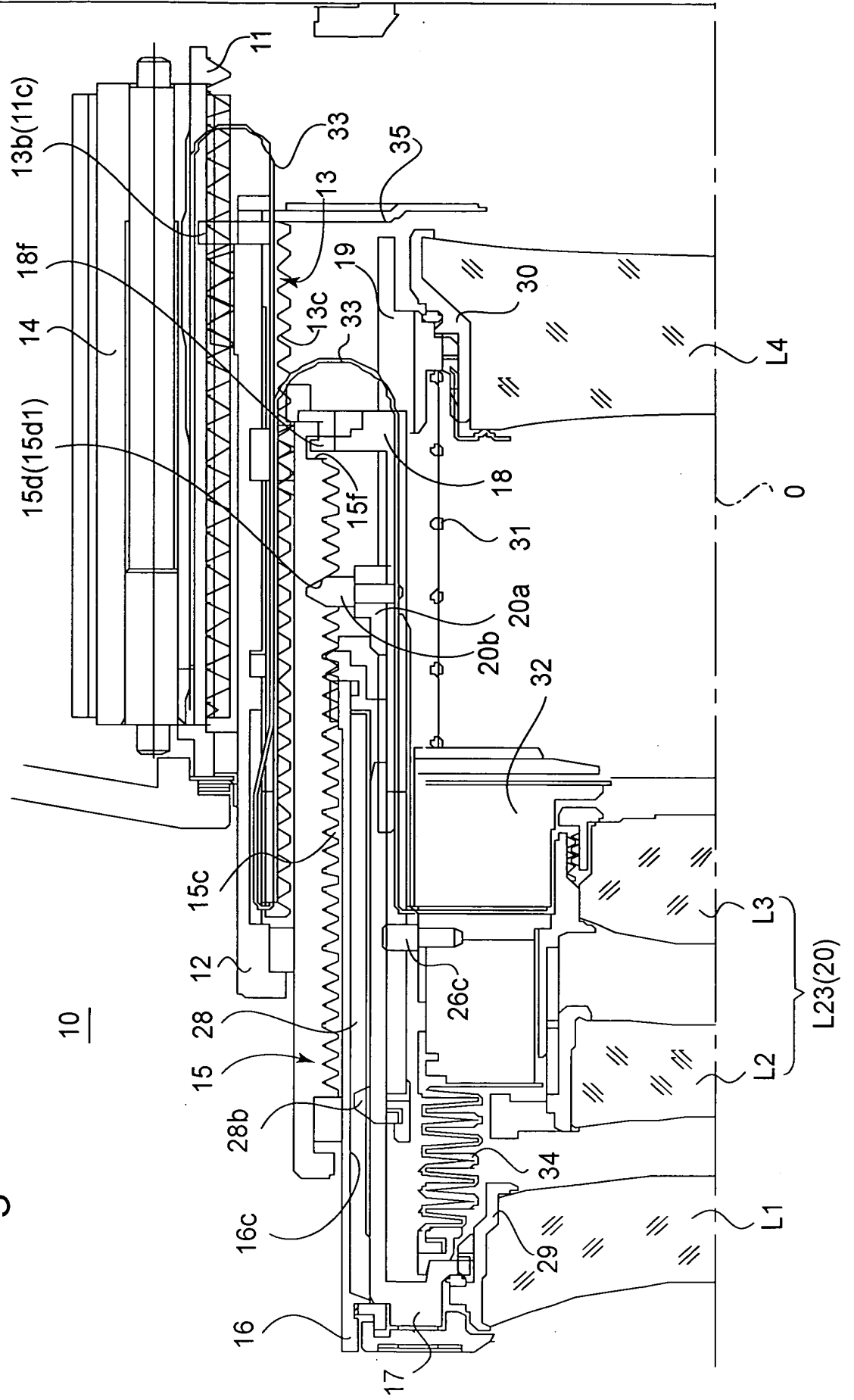




Fig. 6

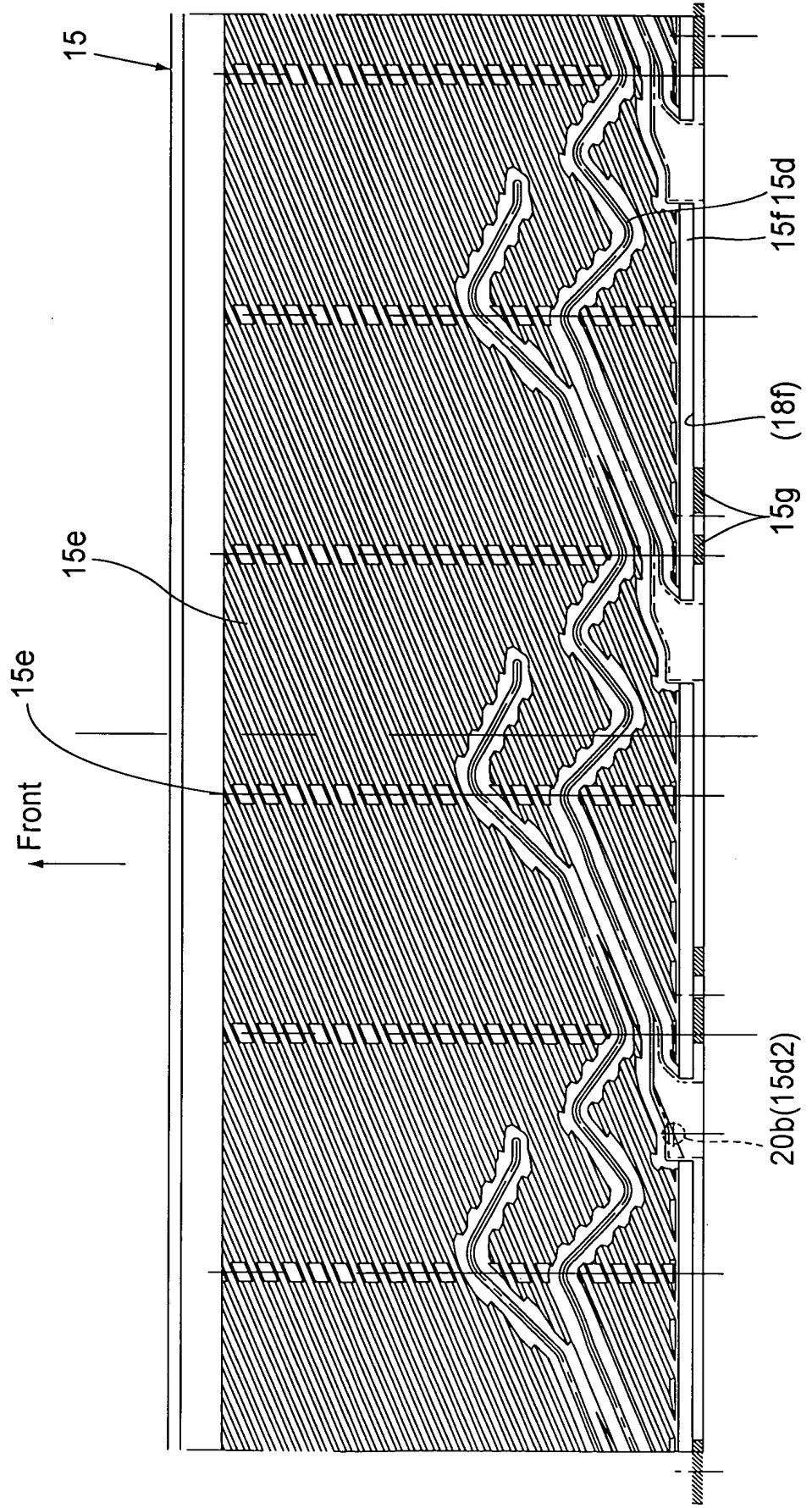


Fig. 7

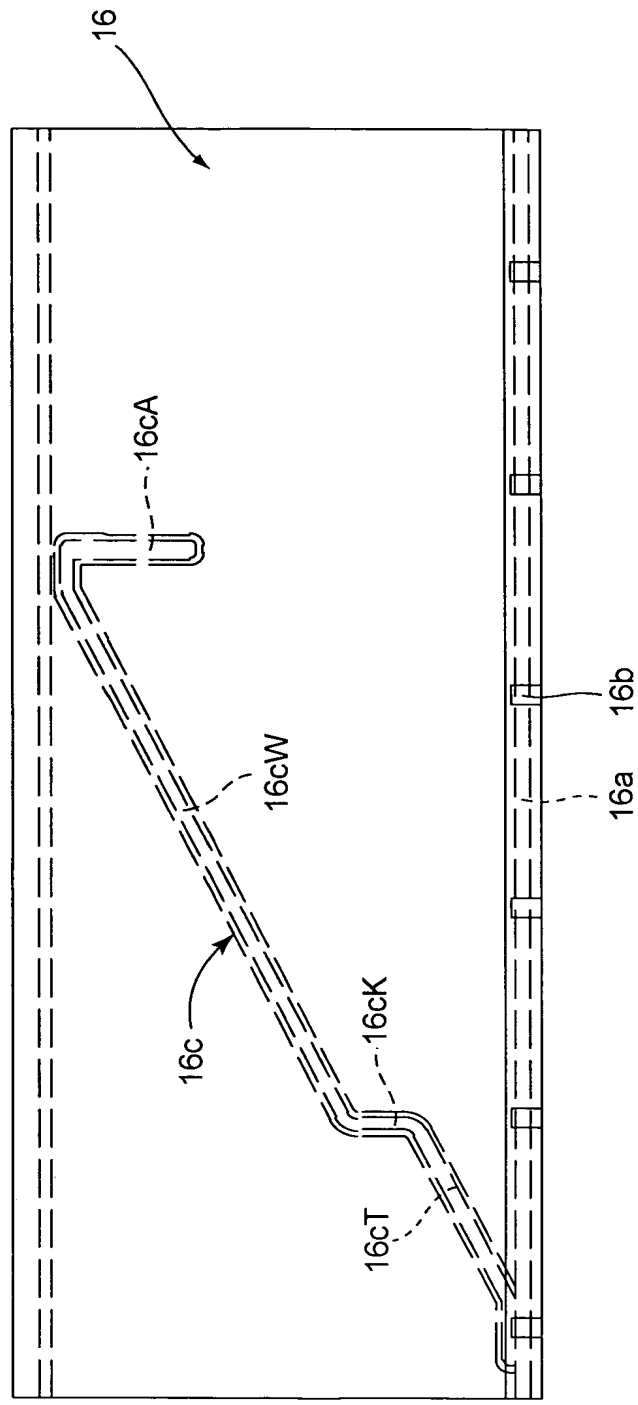




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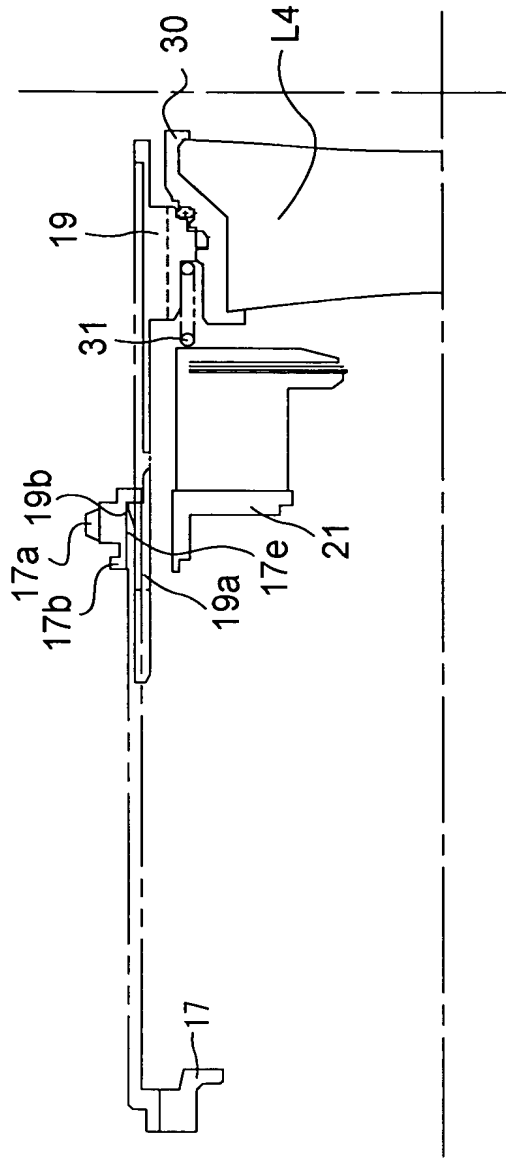


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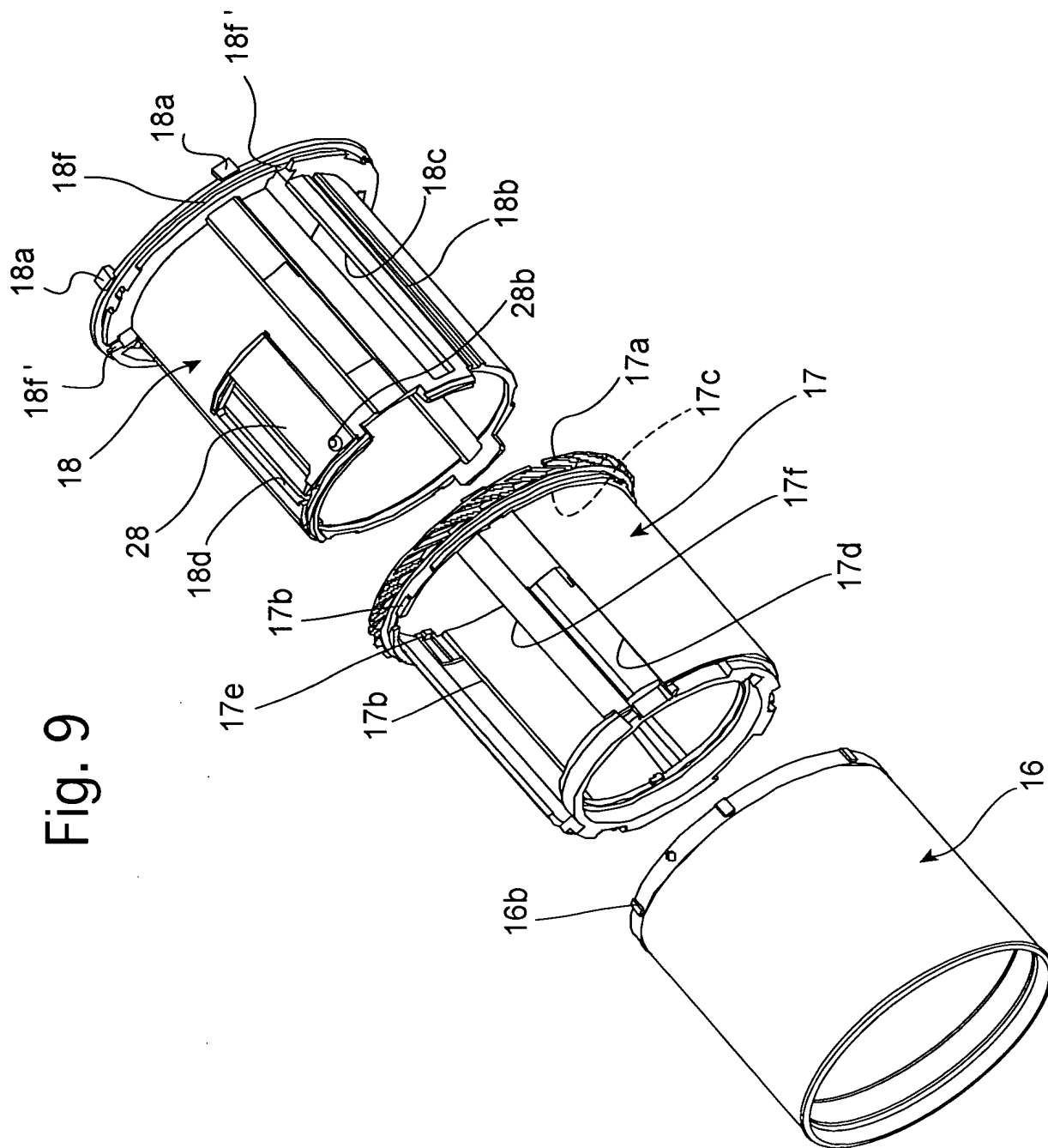


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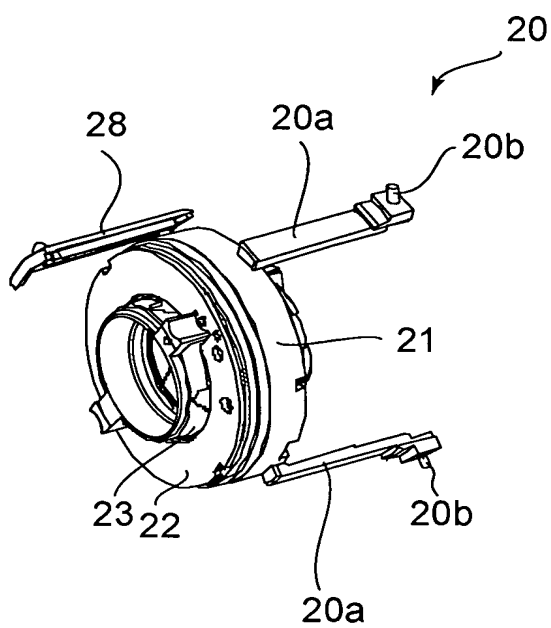


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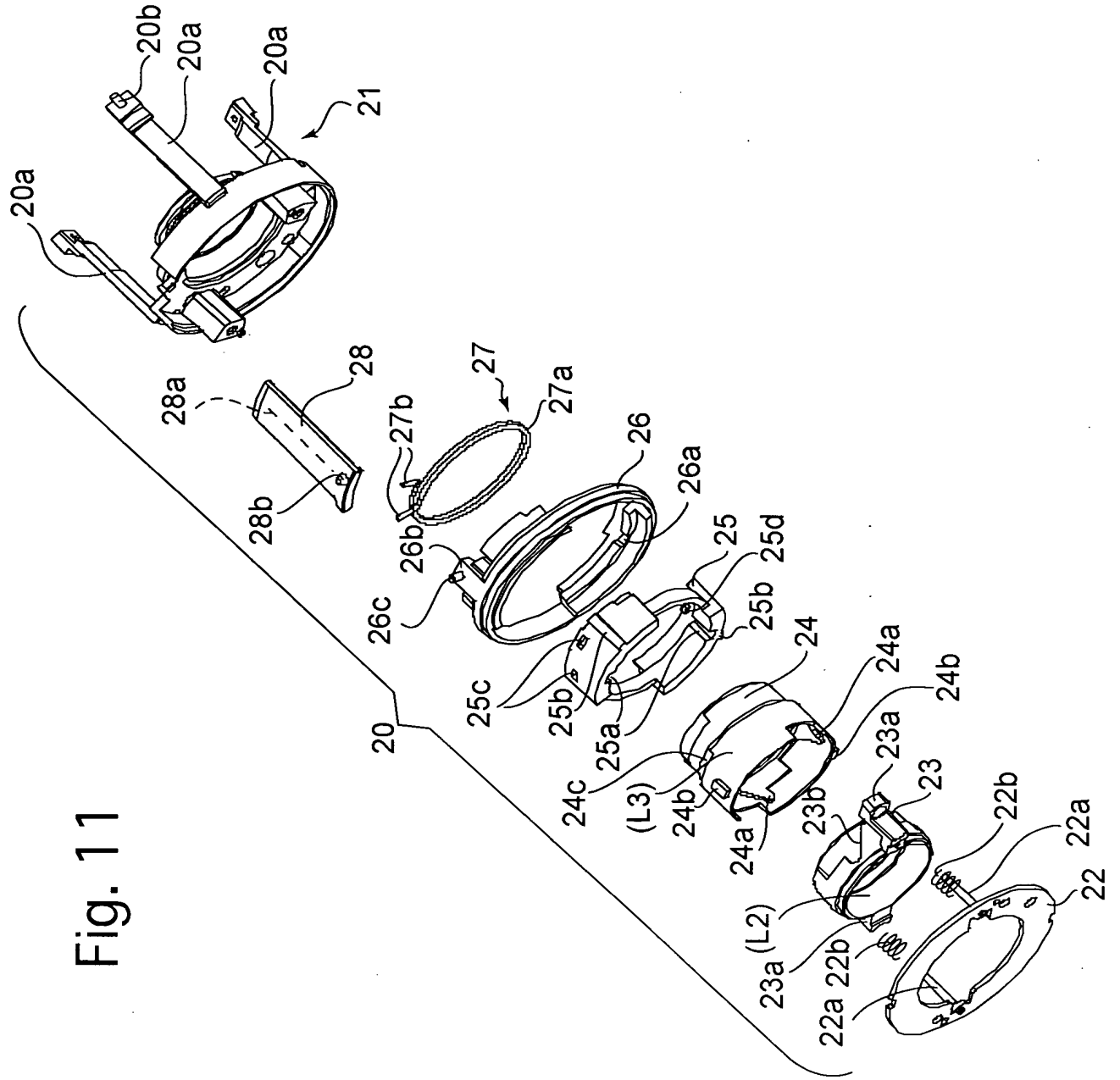


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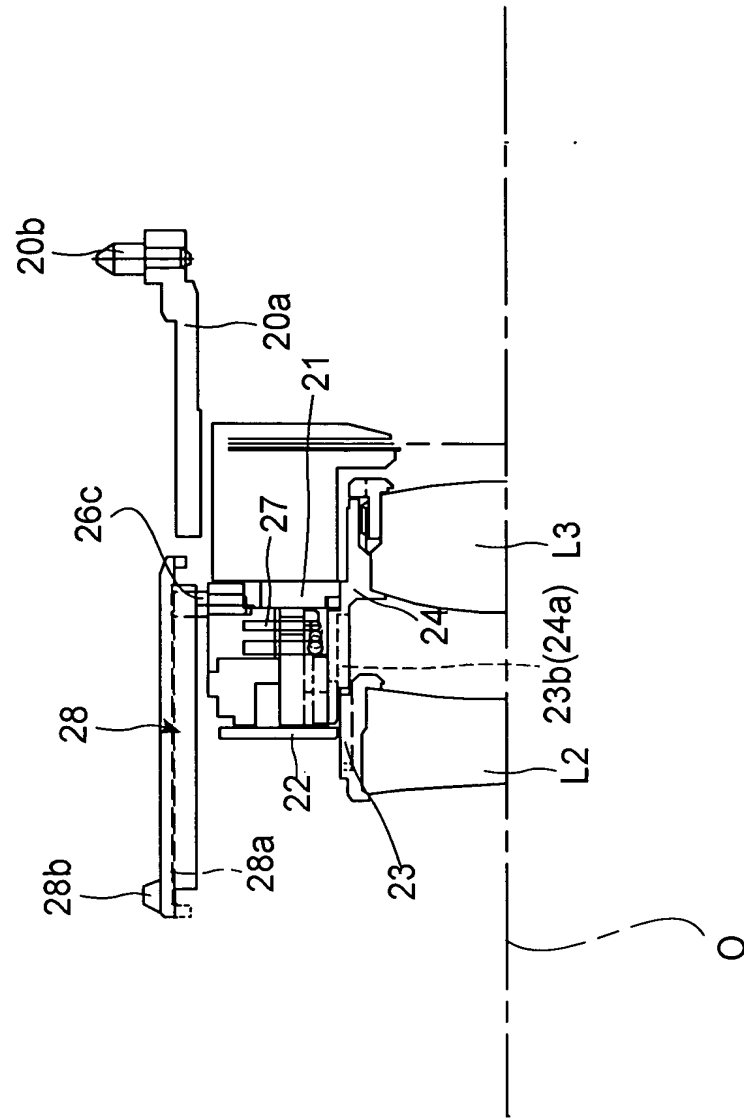


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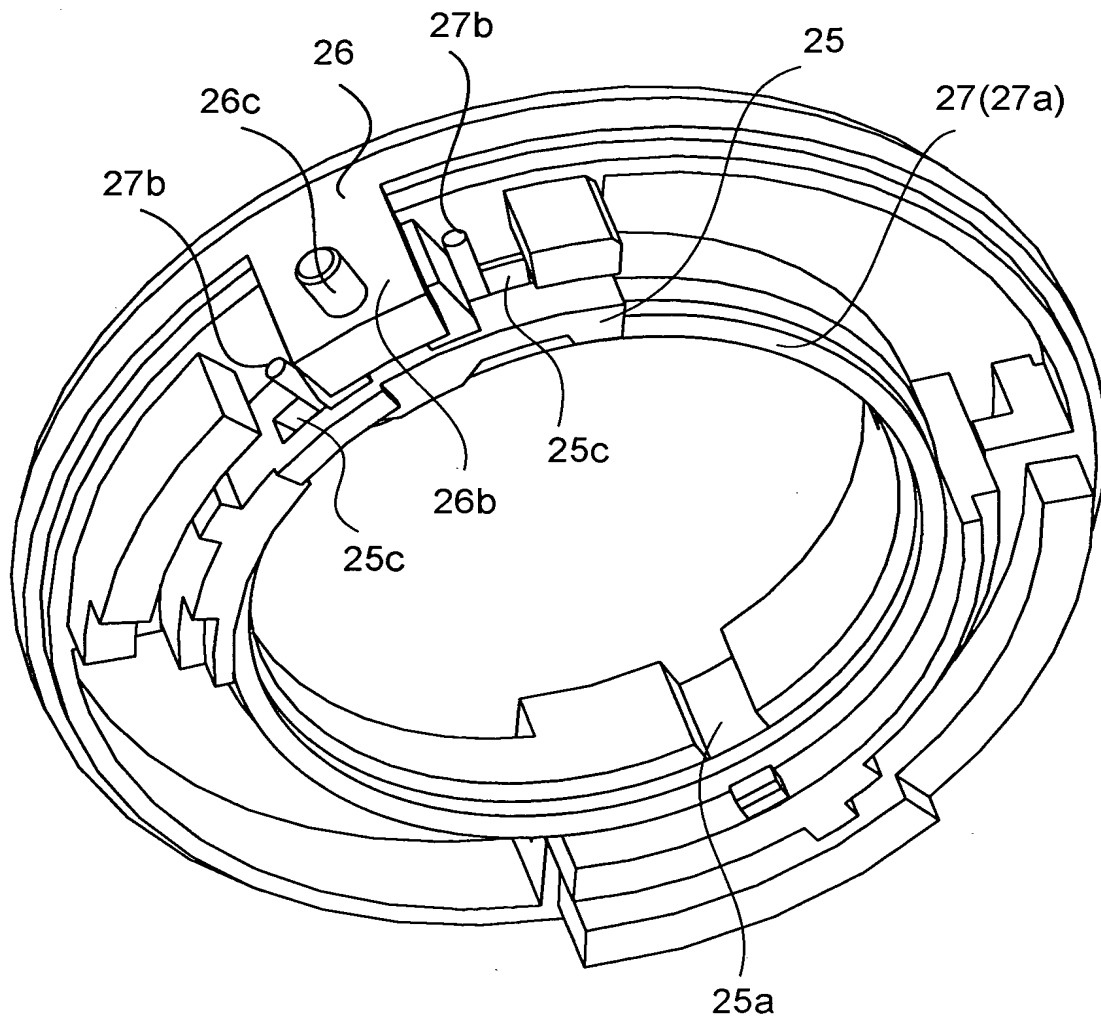


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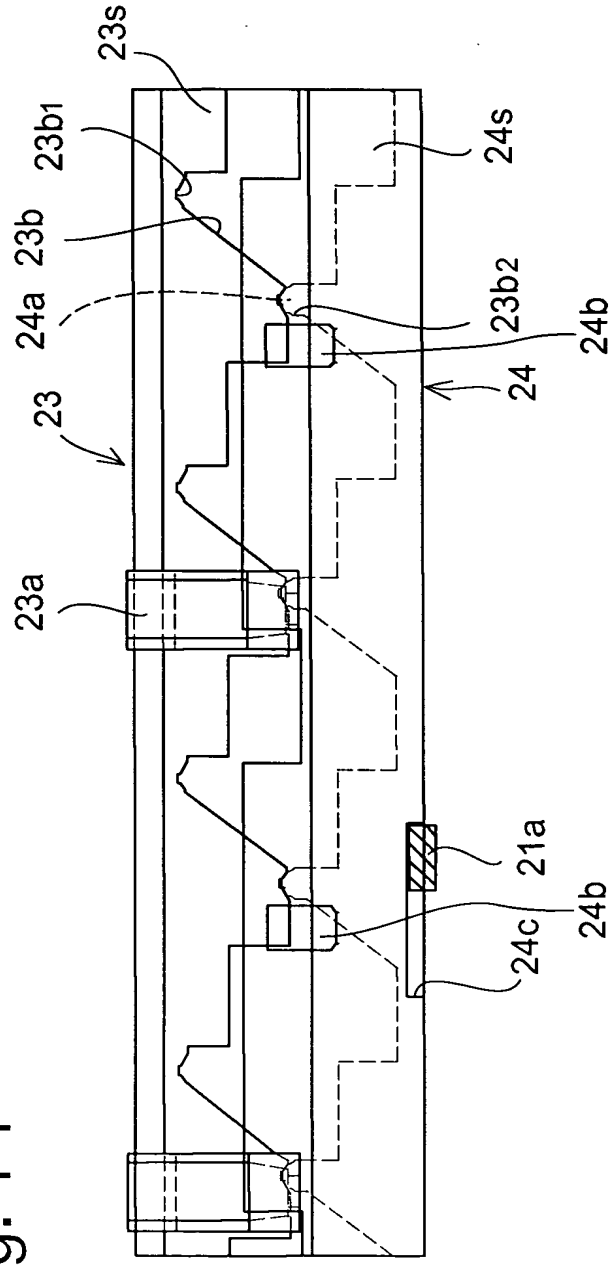


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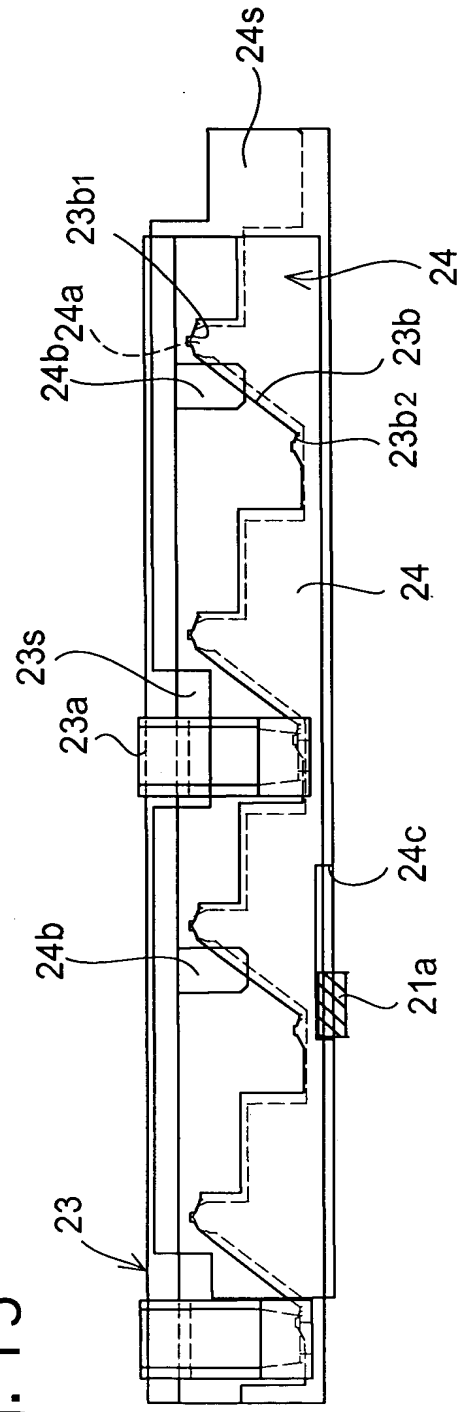


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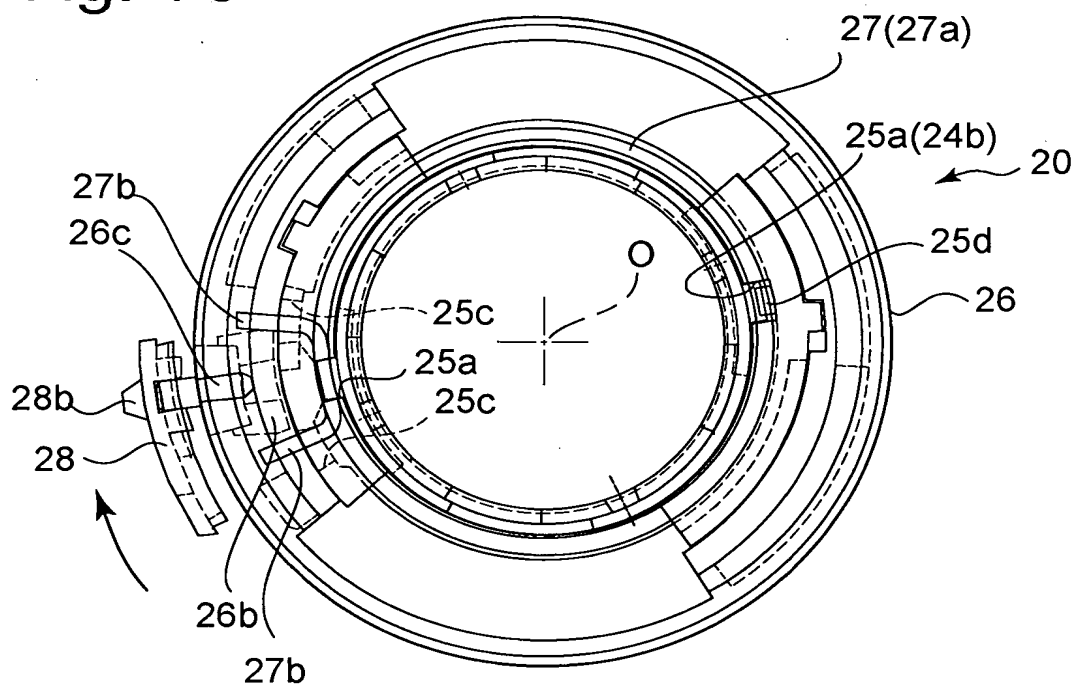
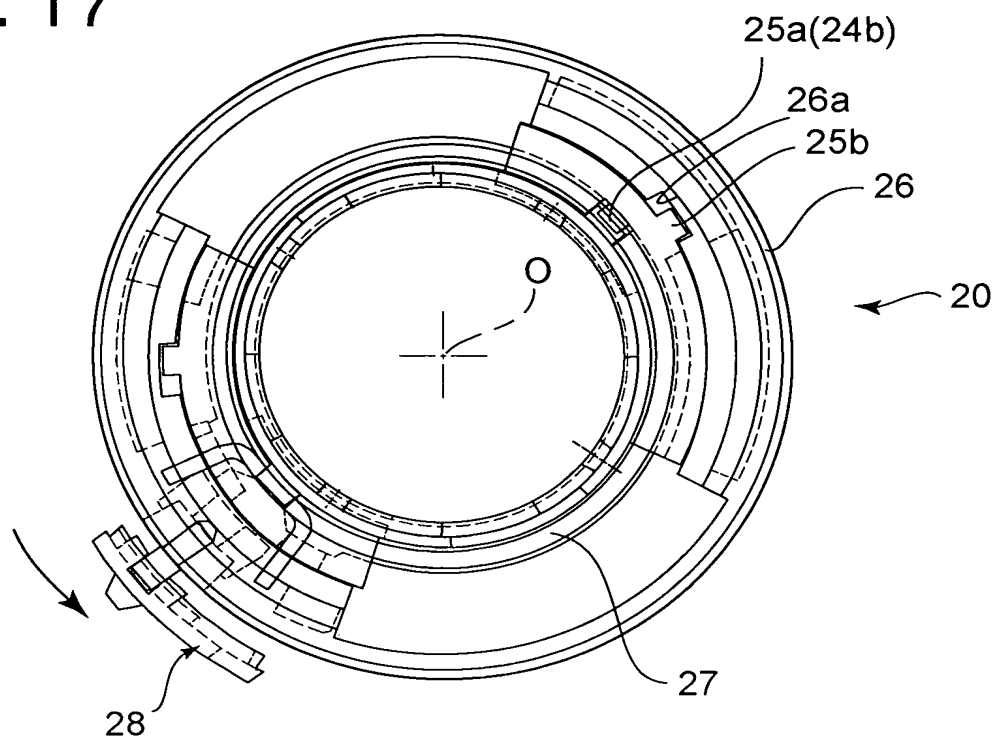


Fig. 17





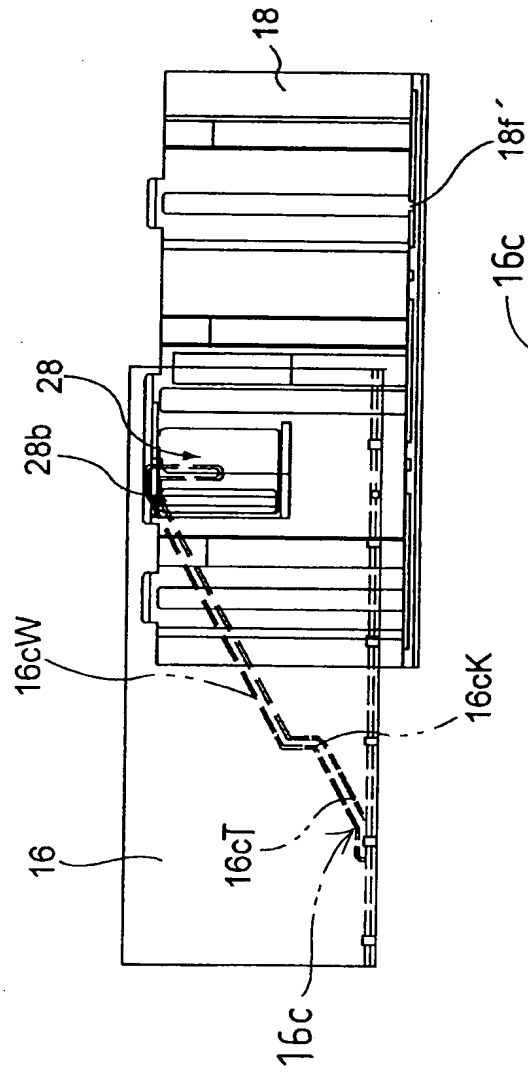


Fig. 18A

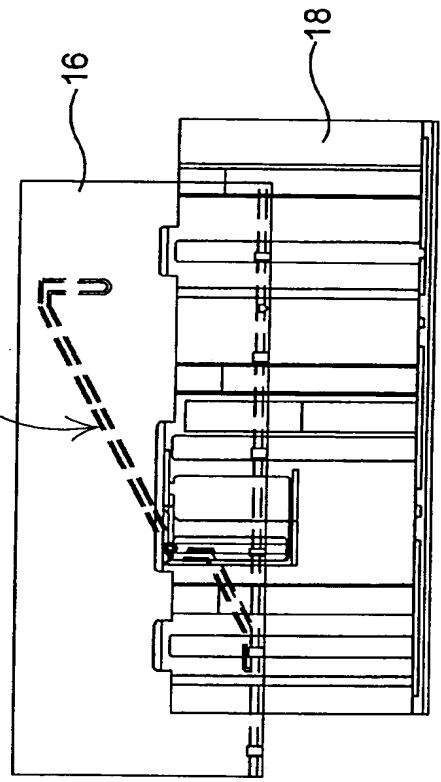


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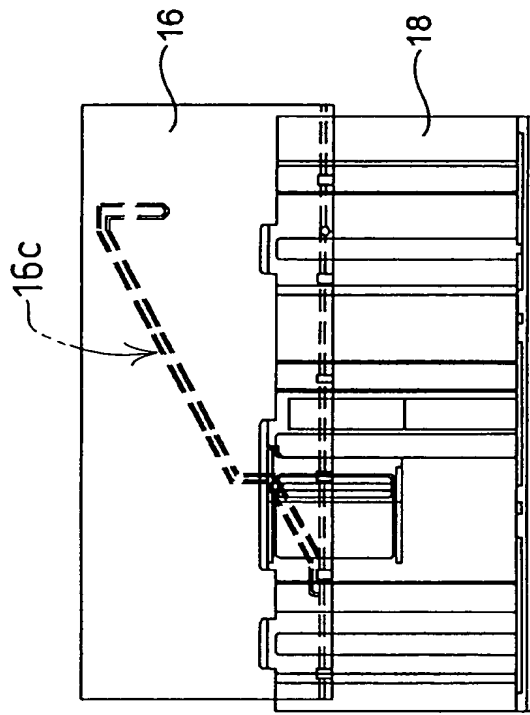


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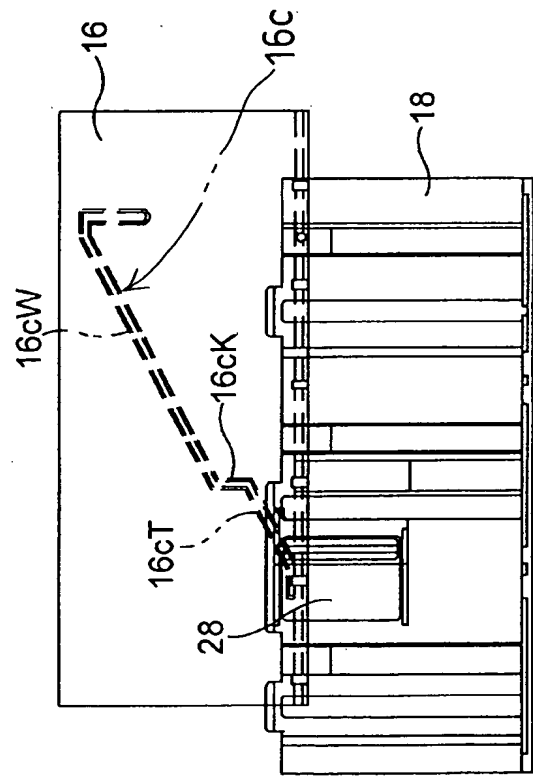


Fig. 18D

Fig. 19

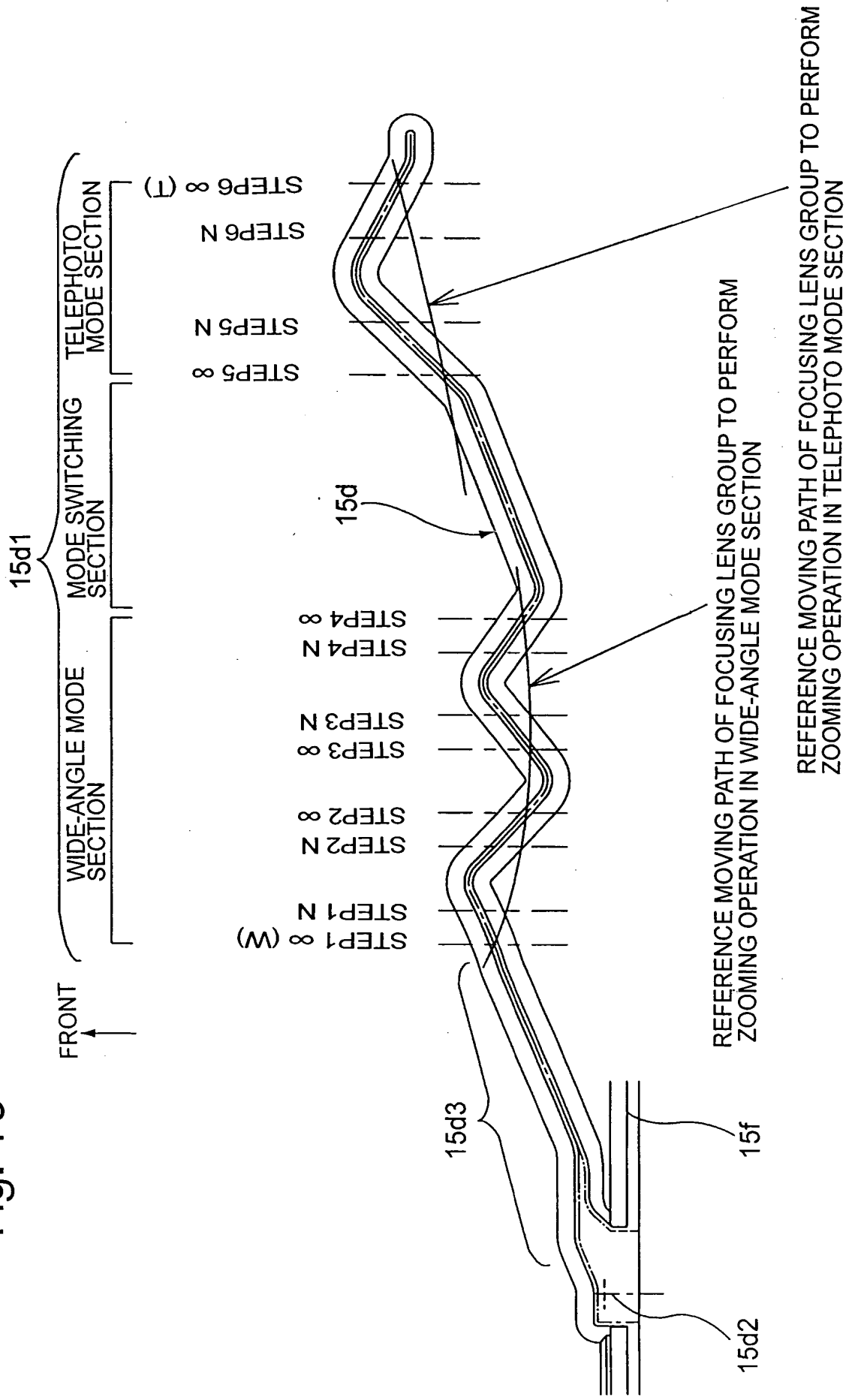


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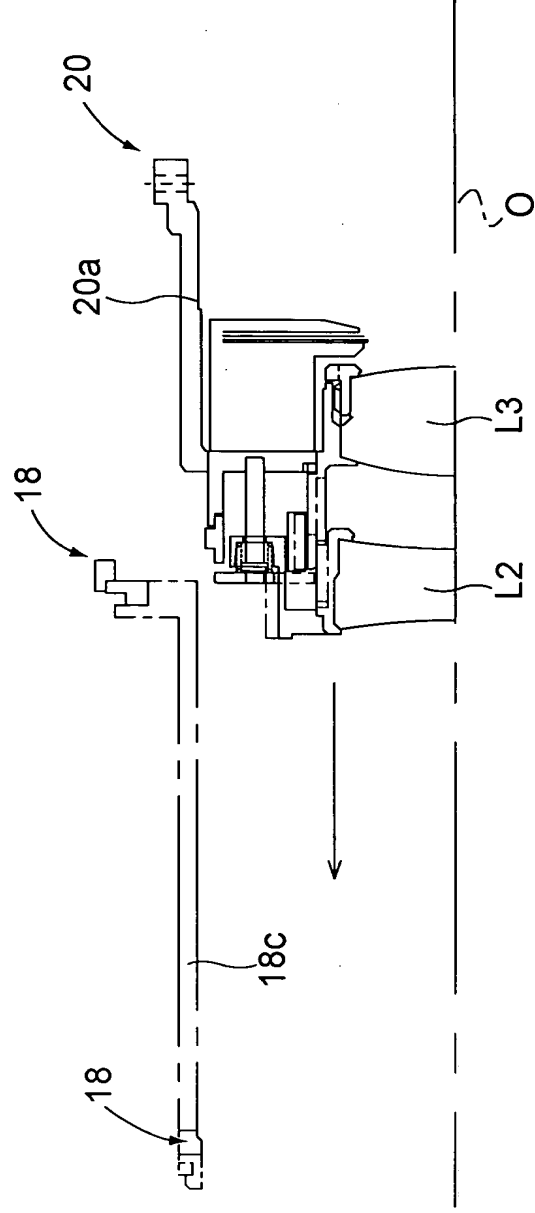


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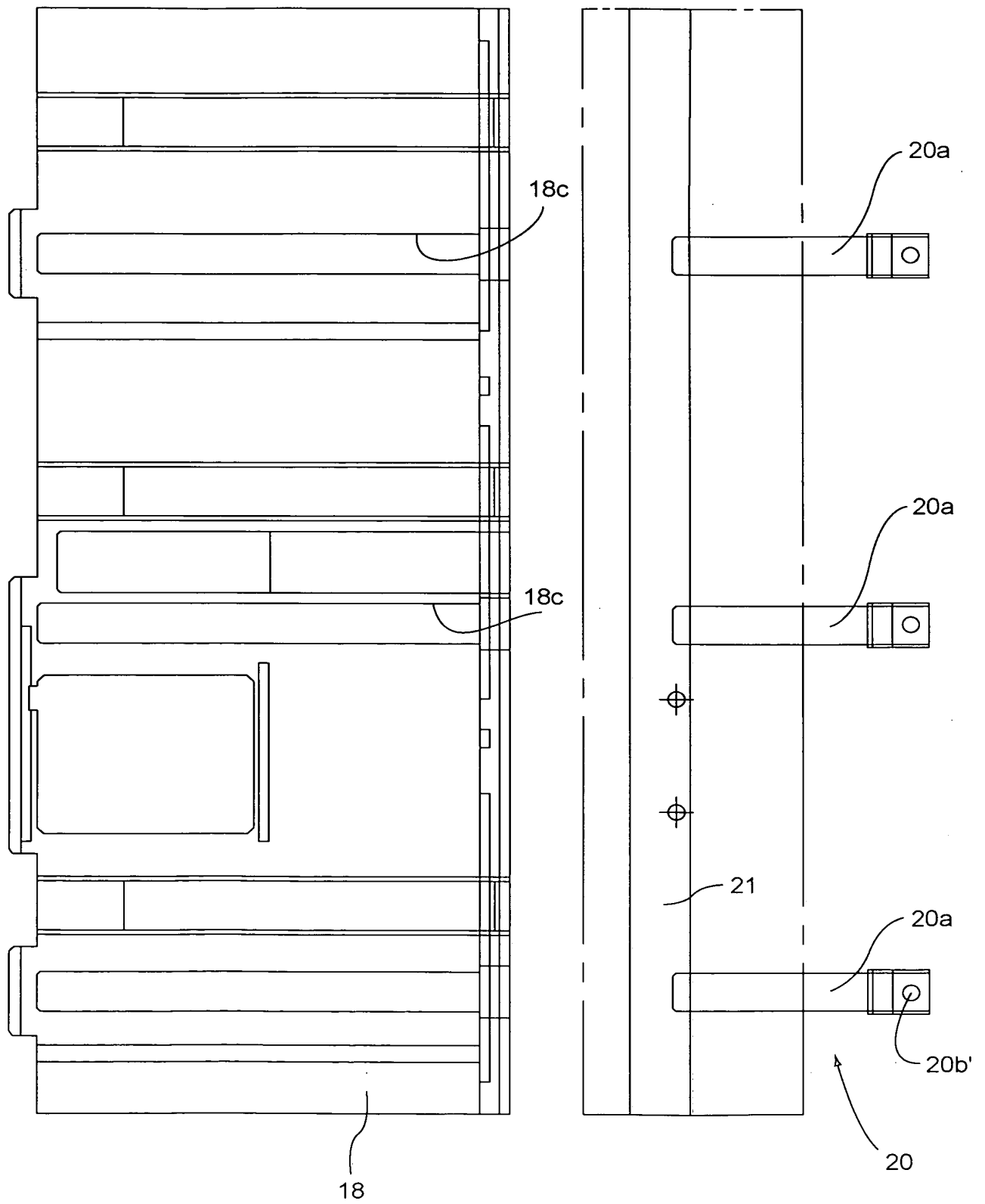


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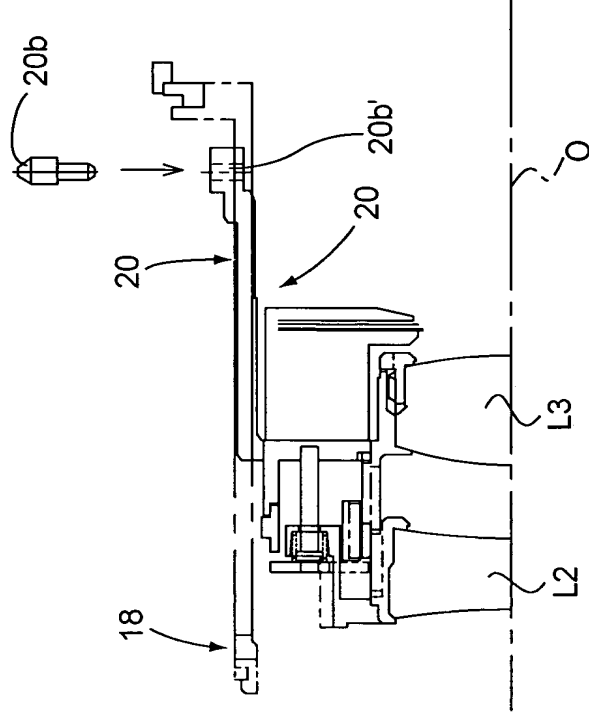


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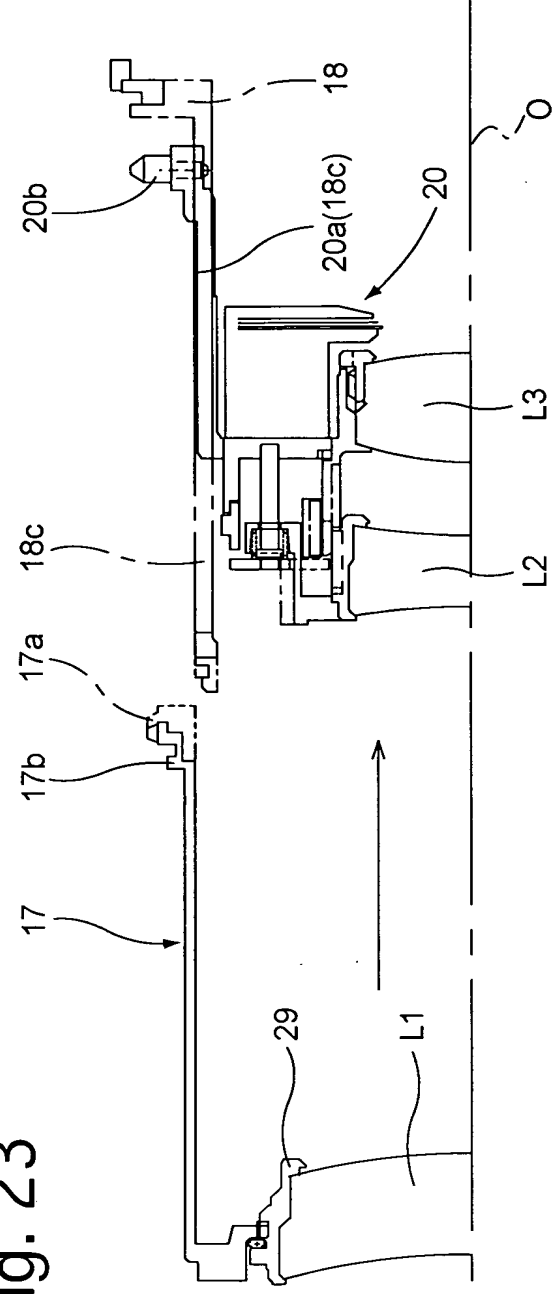


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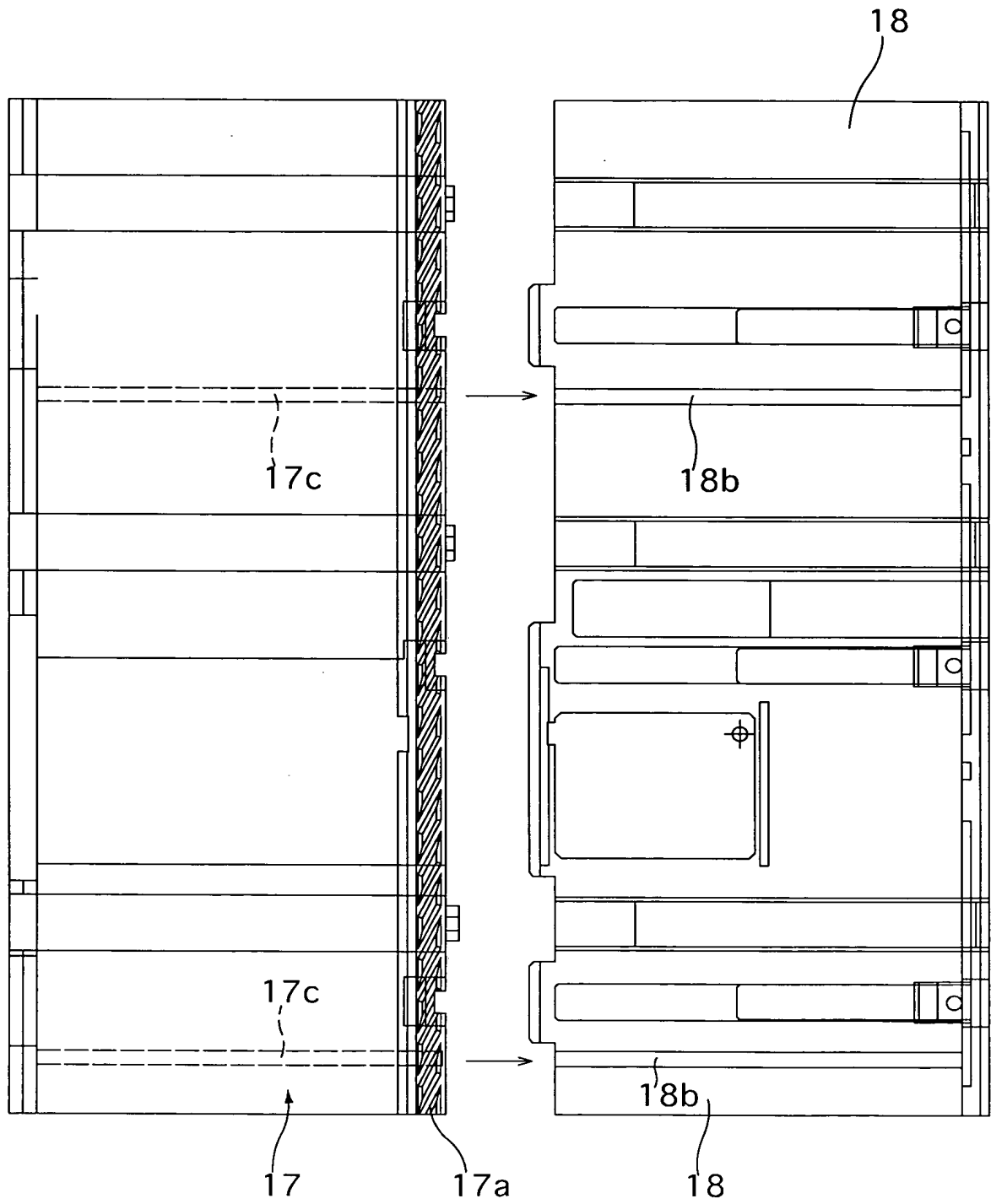


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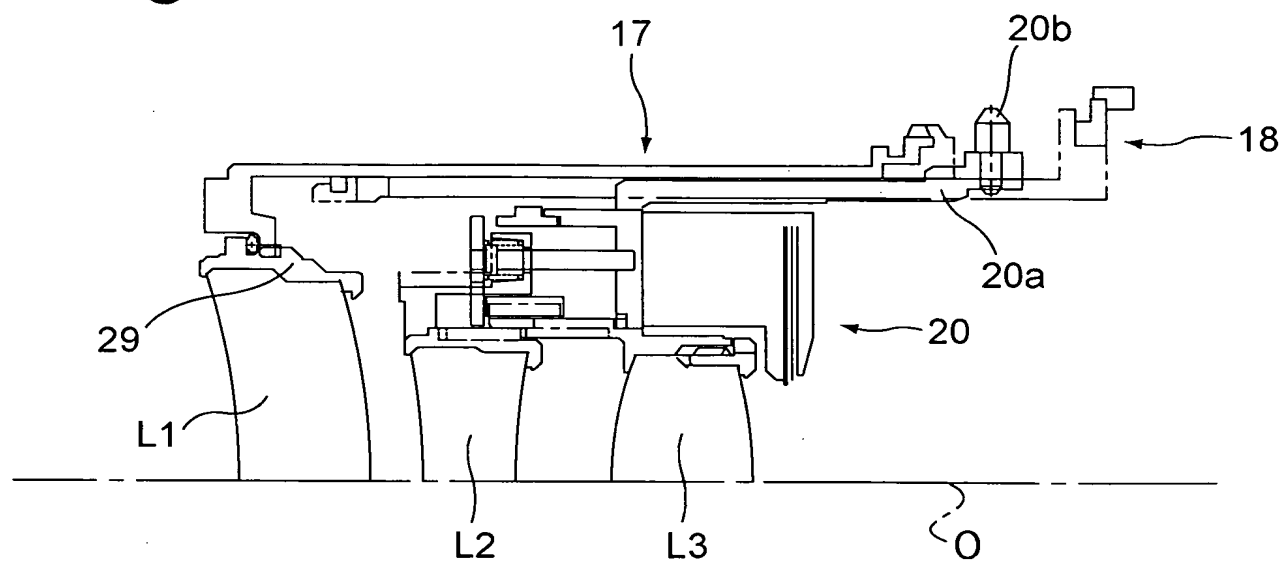


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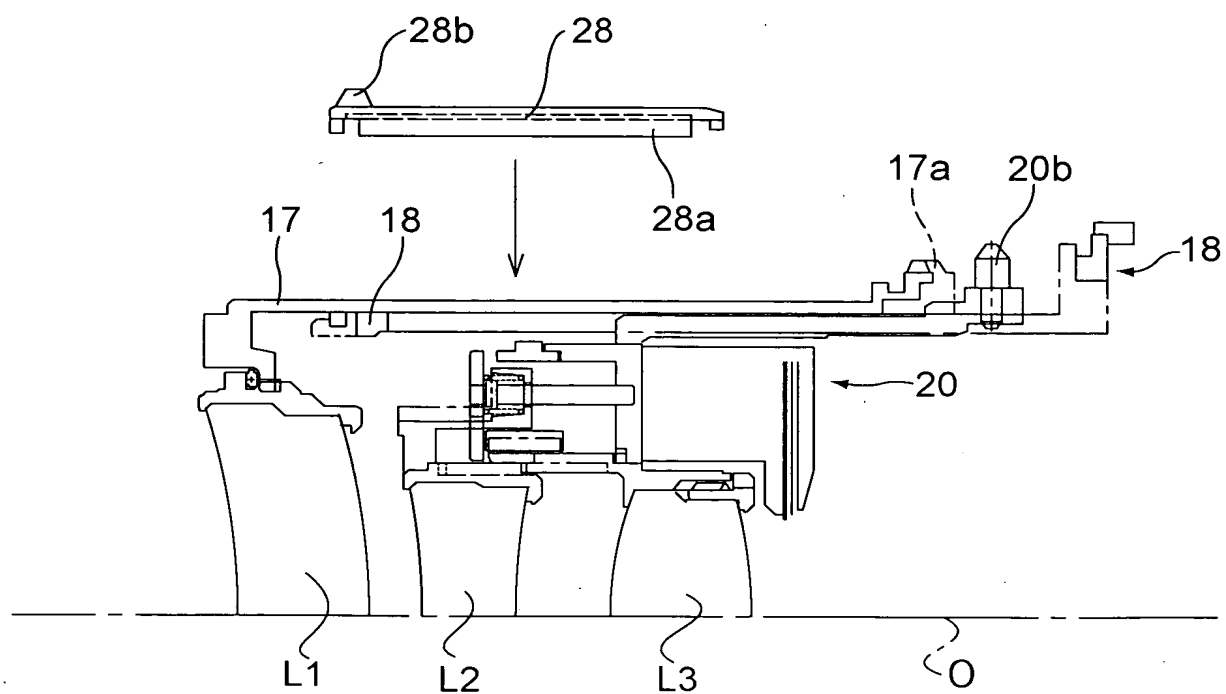




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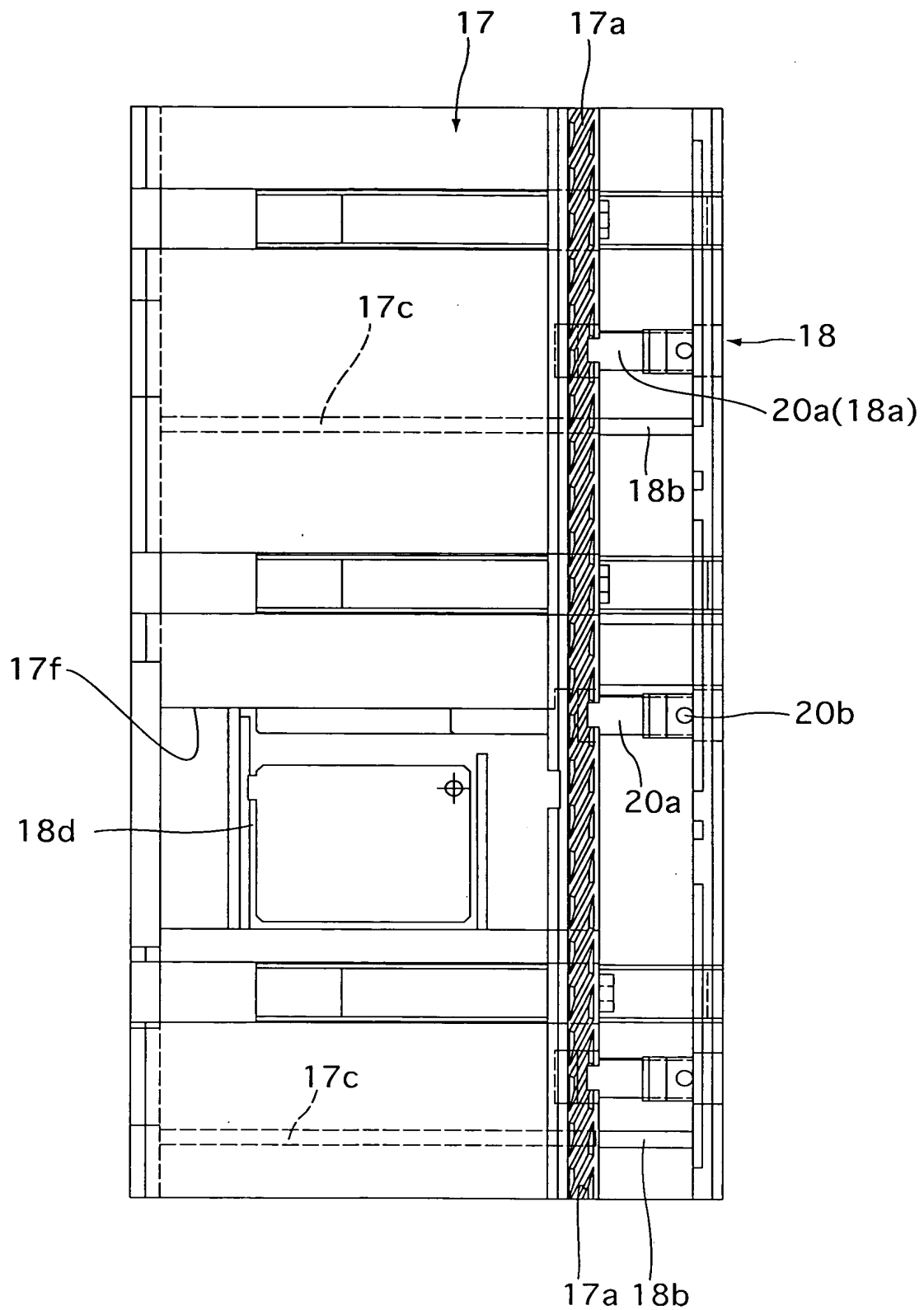


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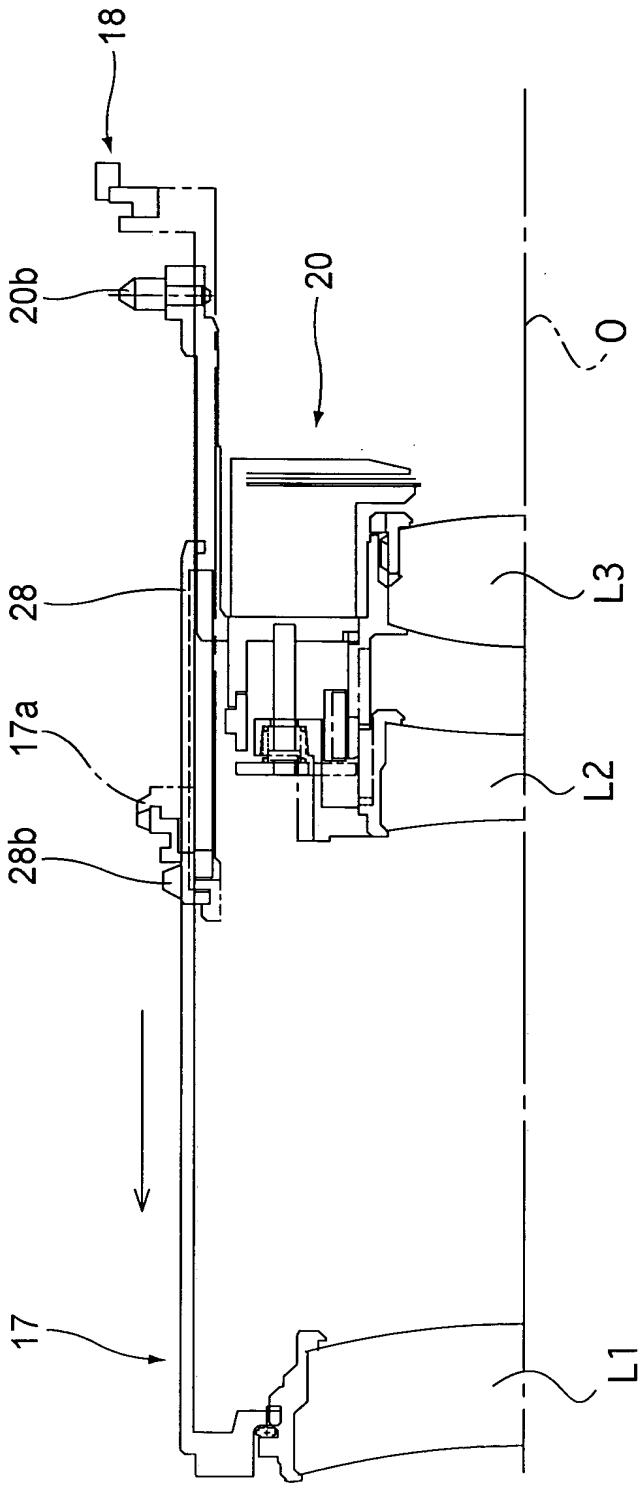




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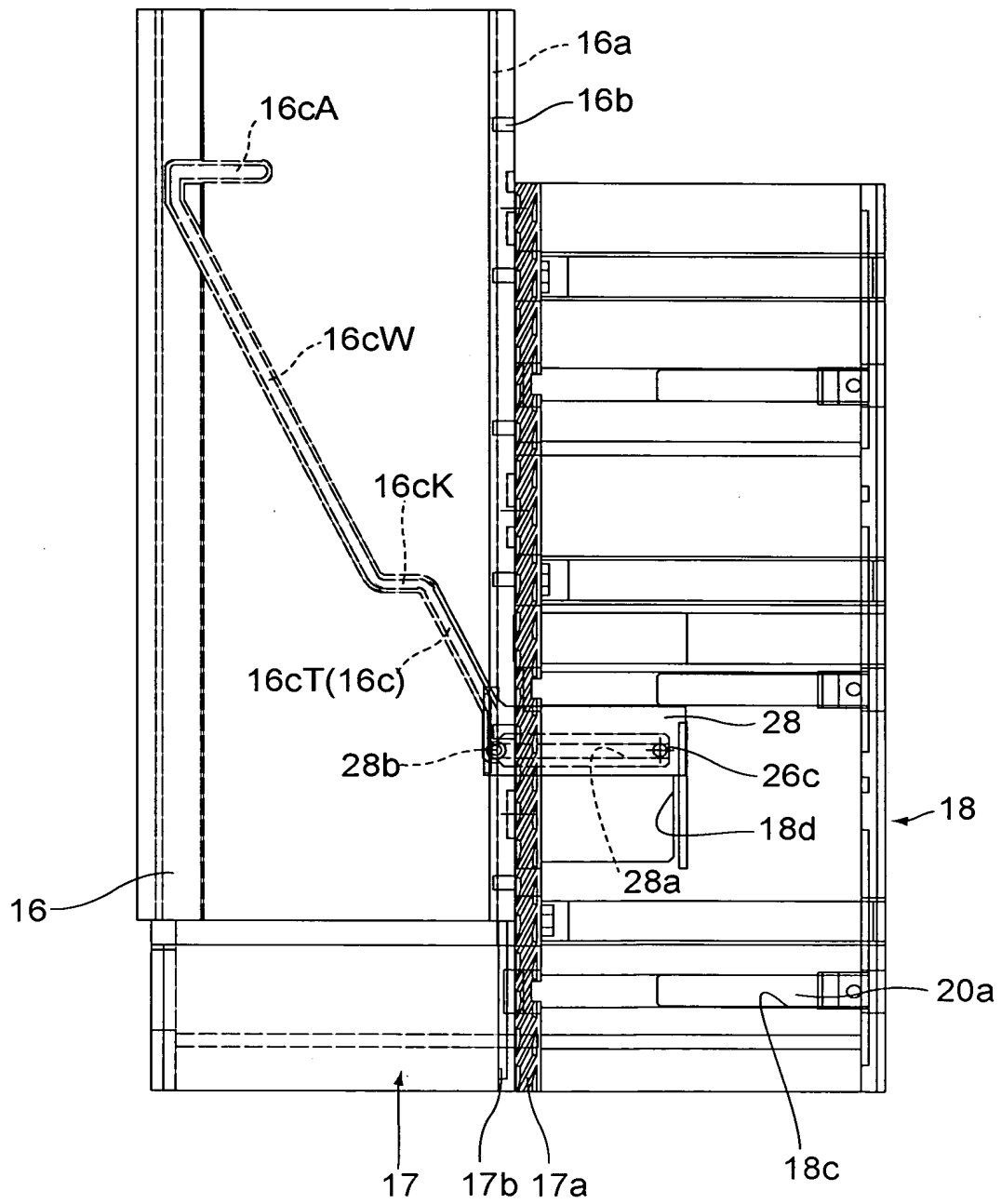


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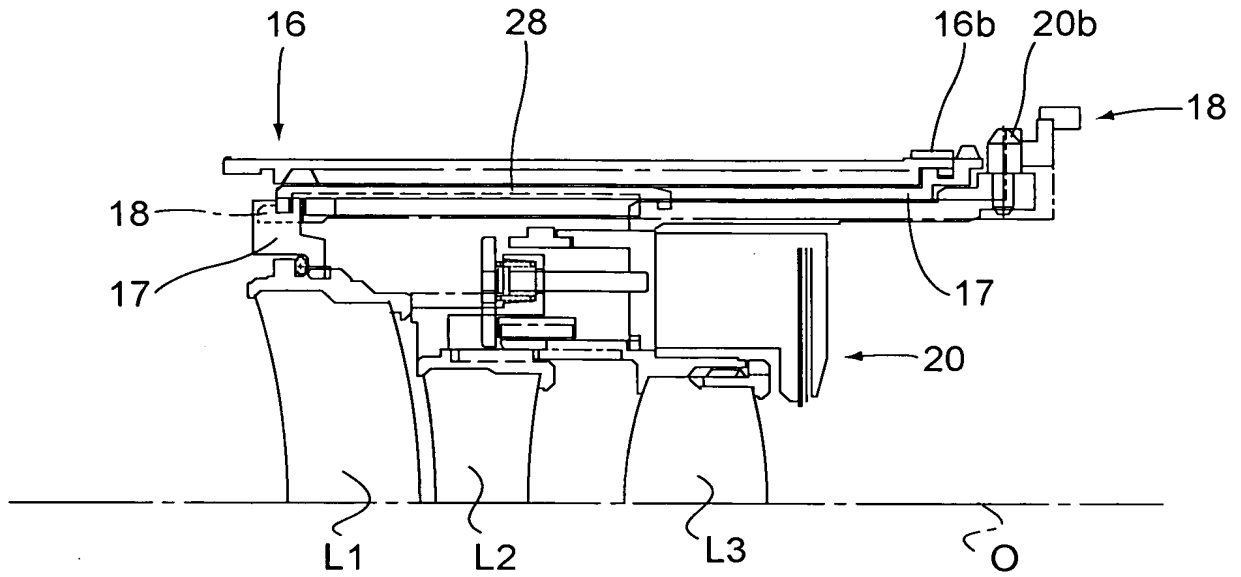


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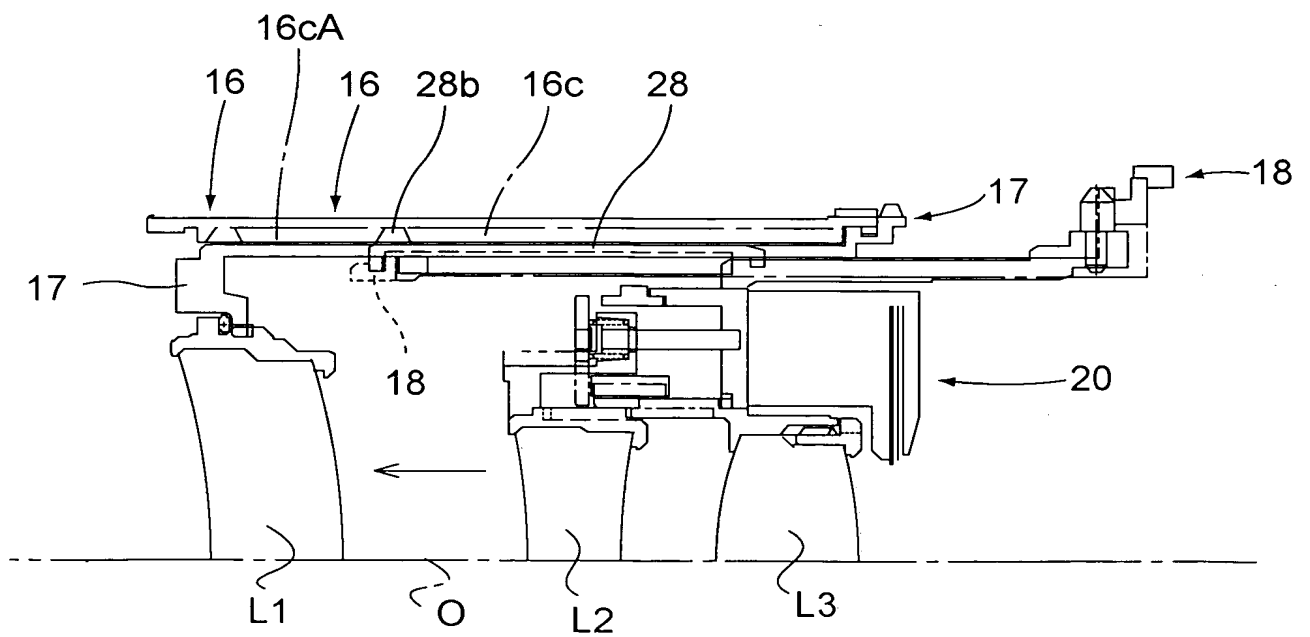


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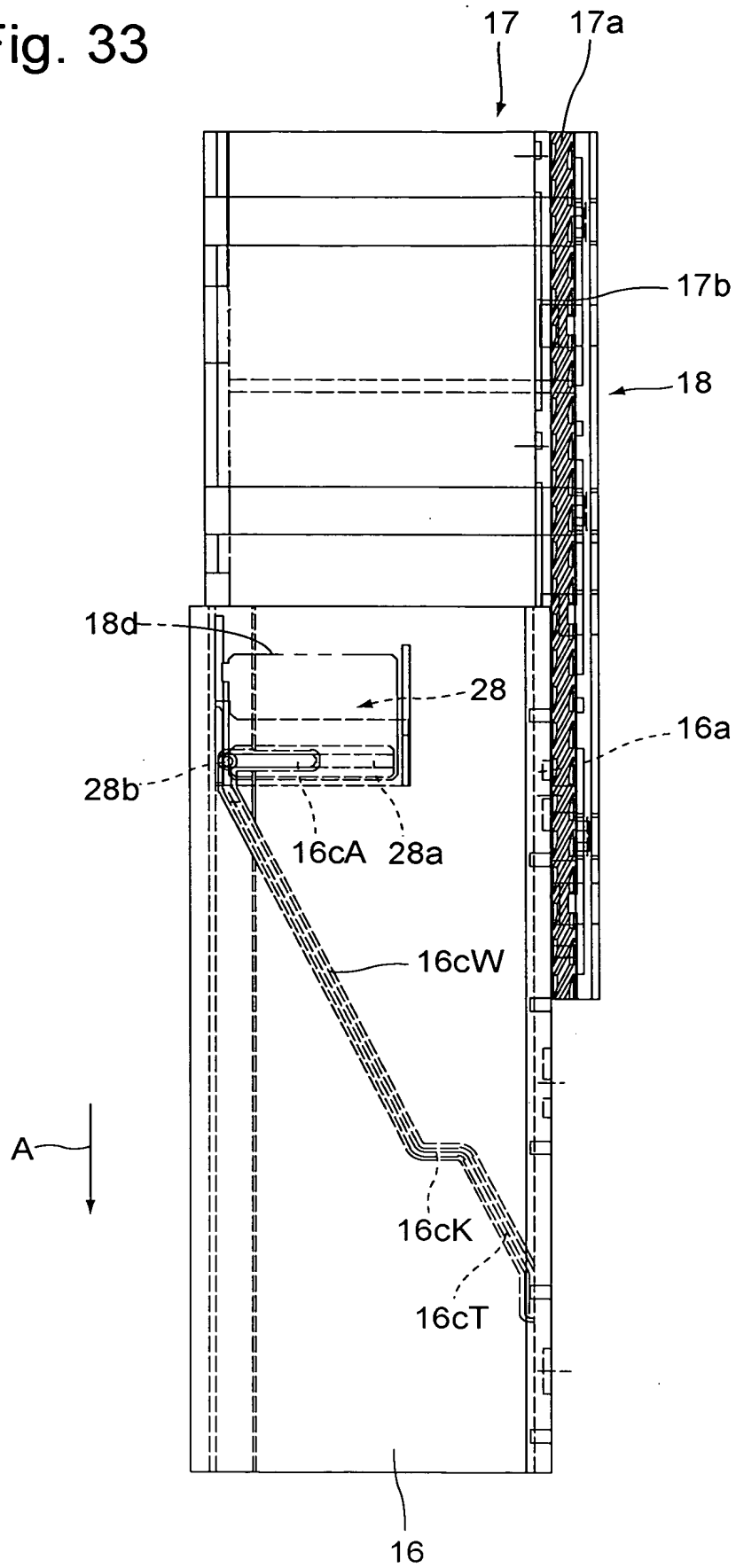


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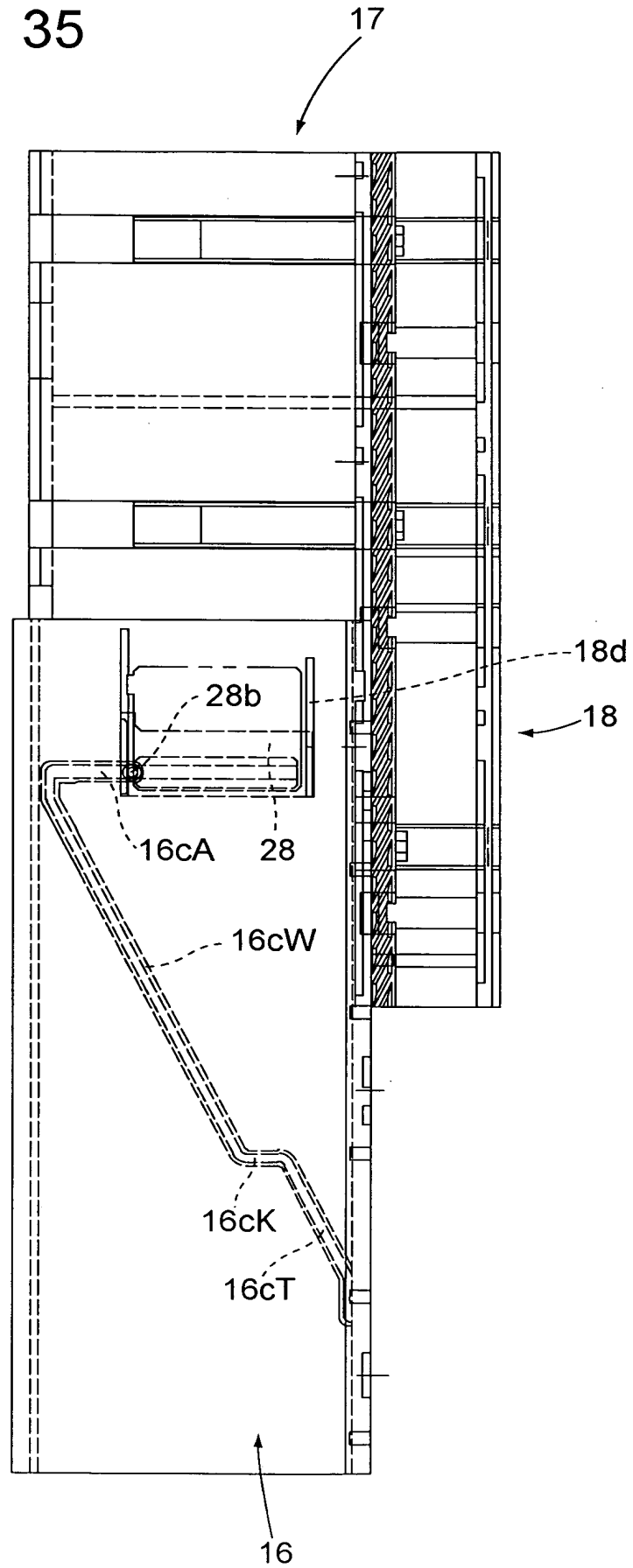


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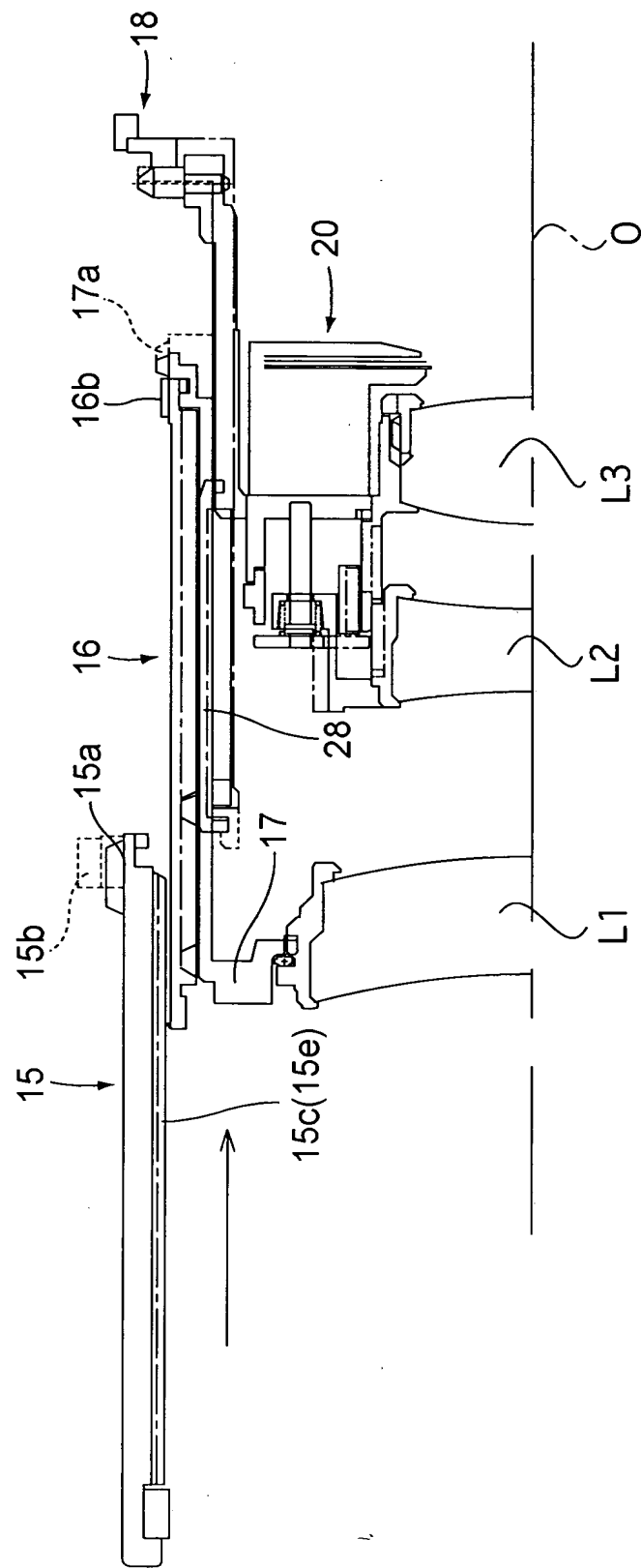




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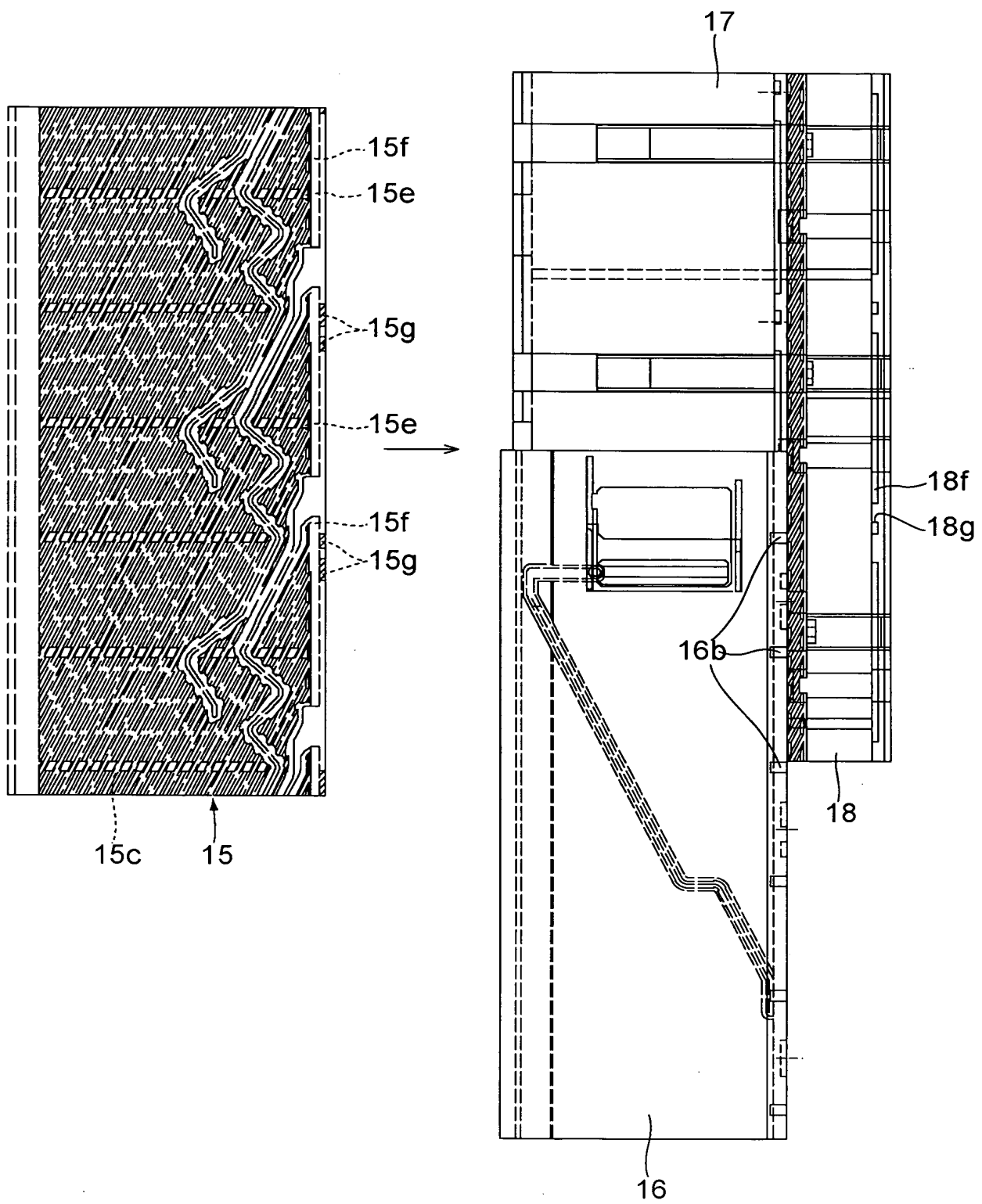


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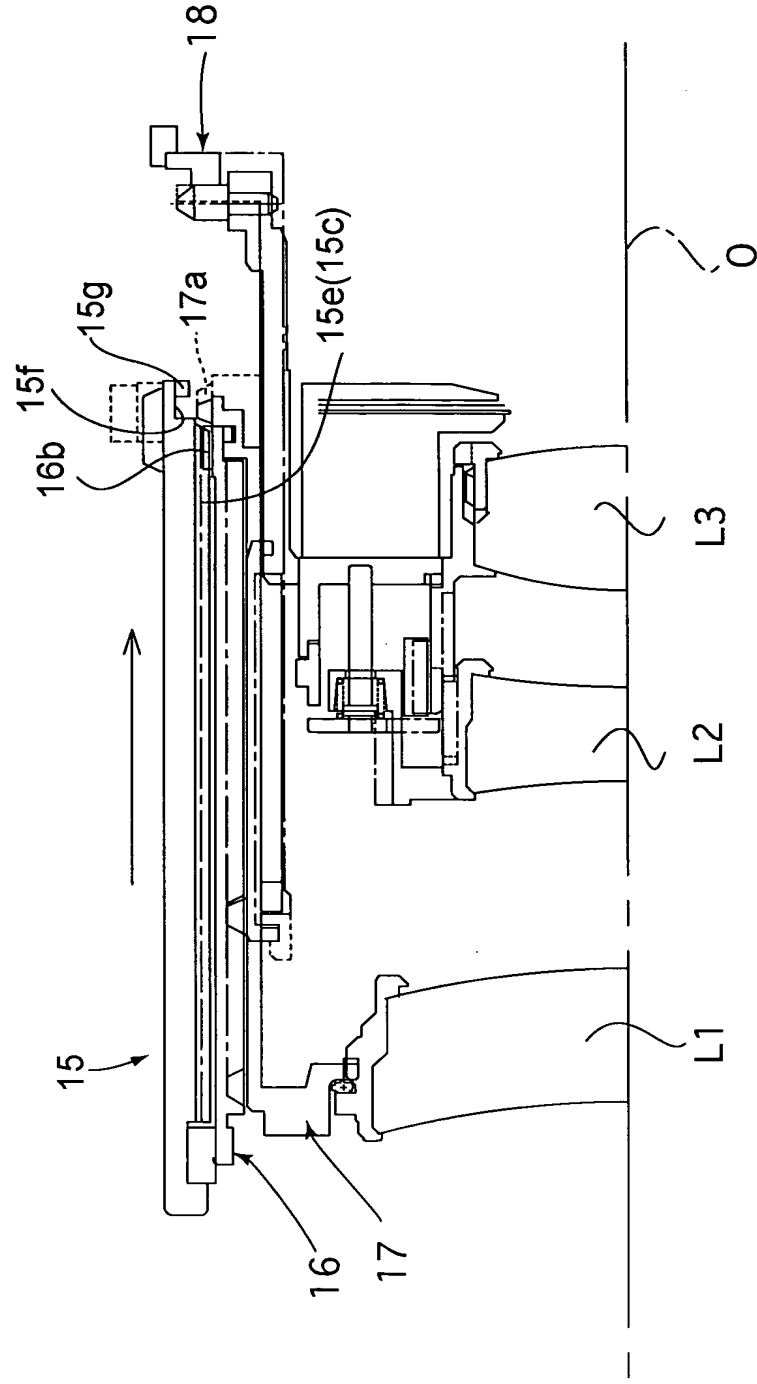


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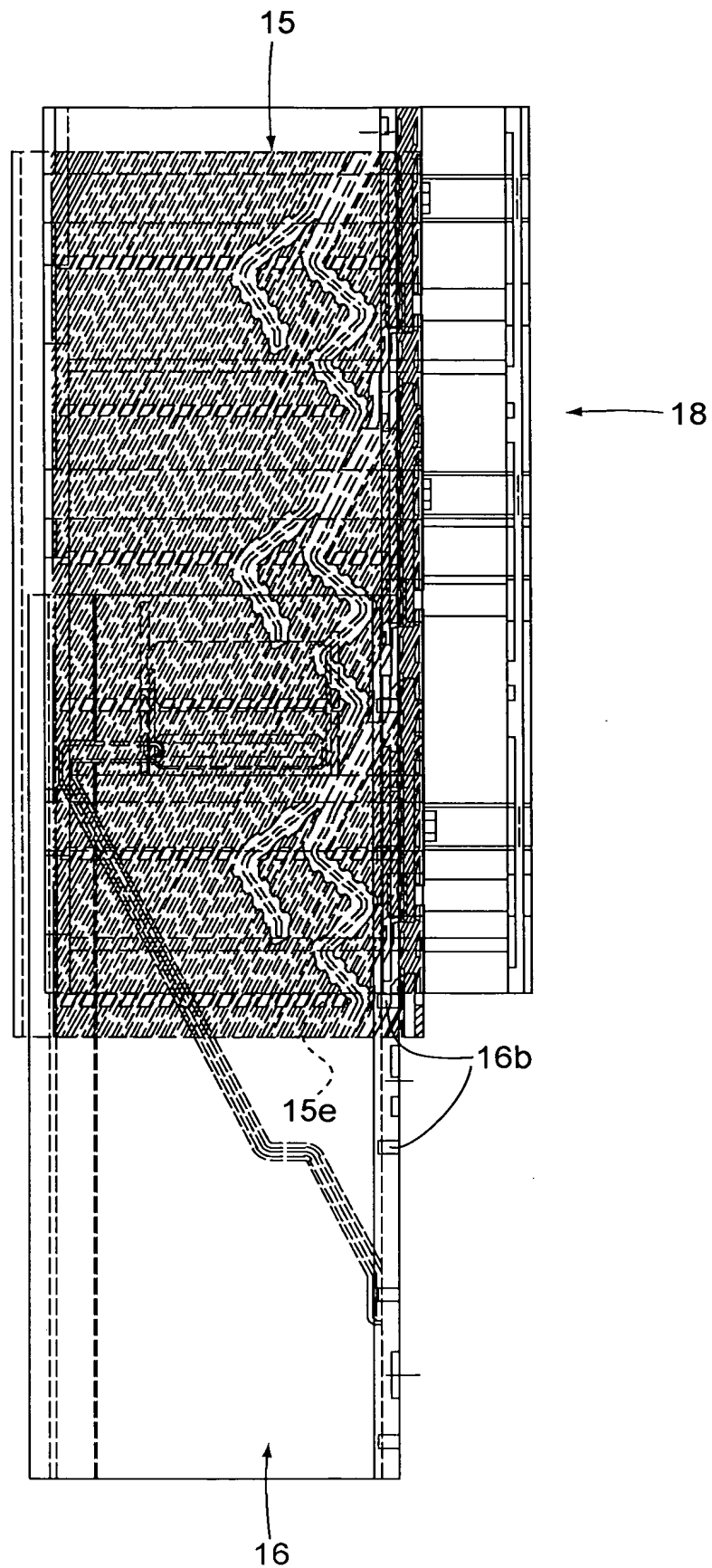


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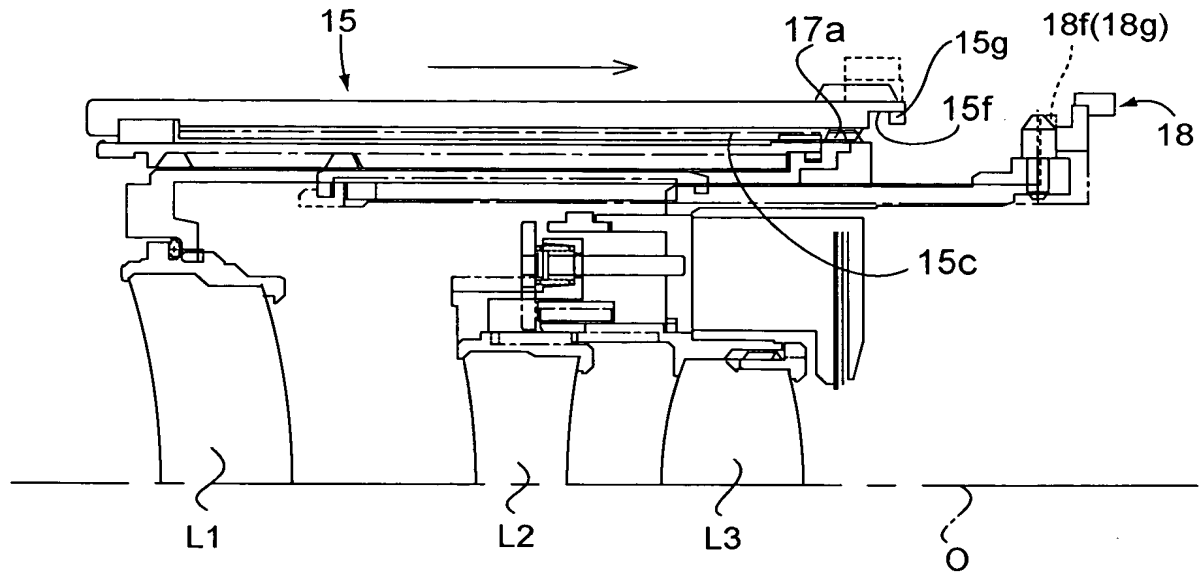


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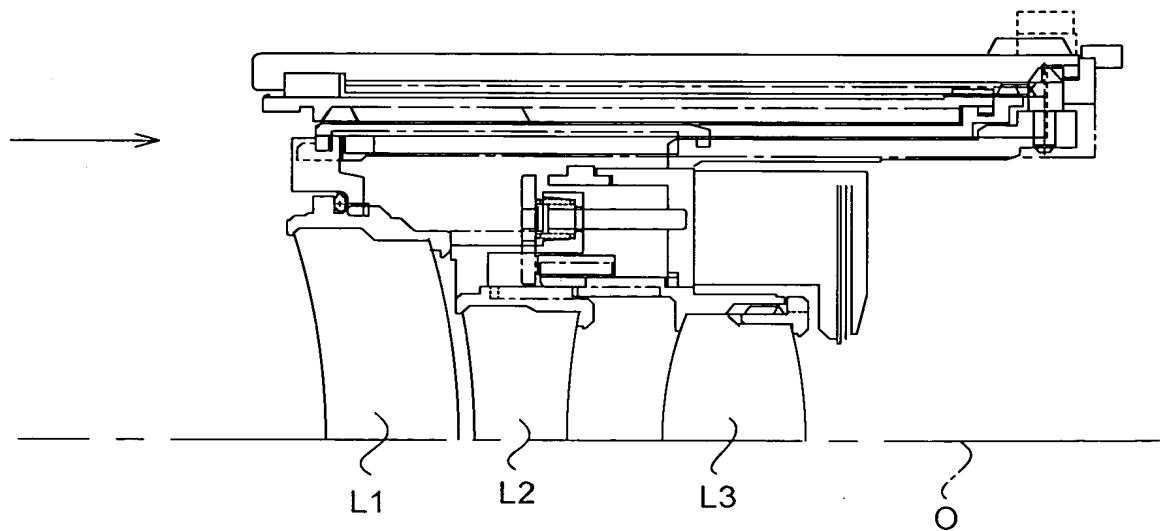


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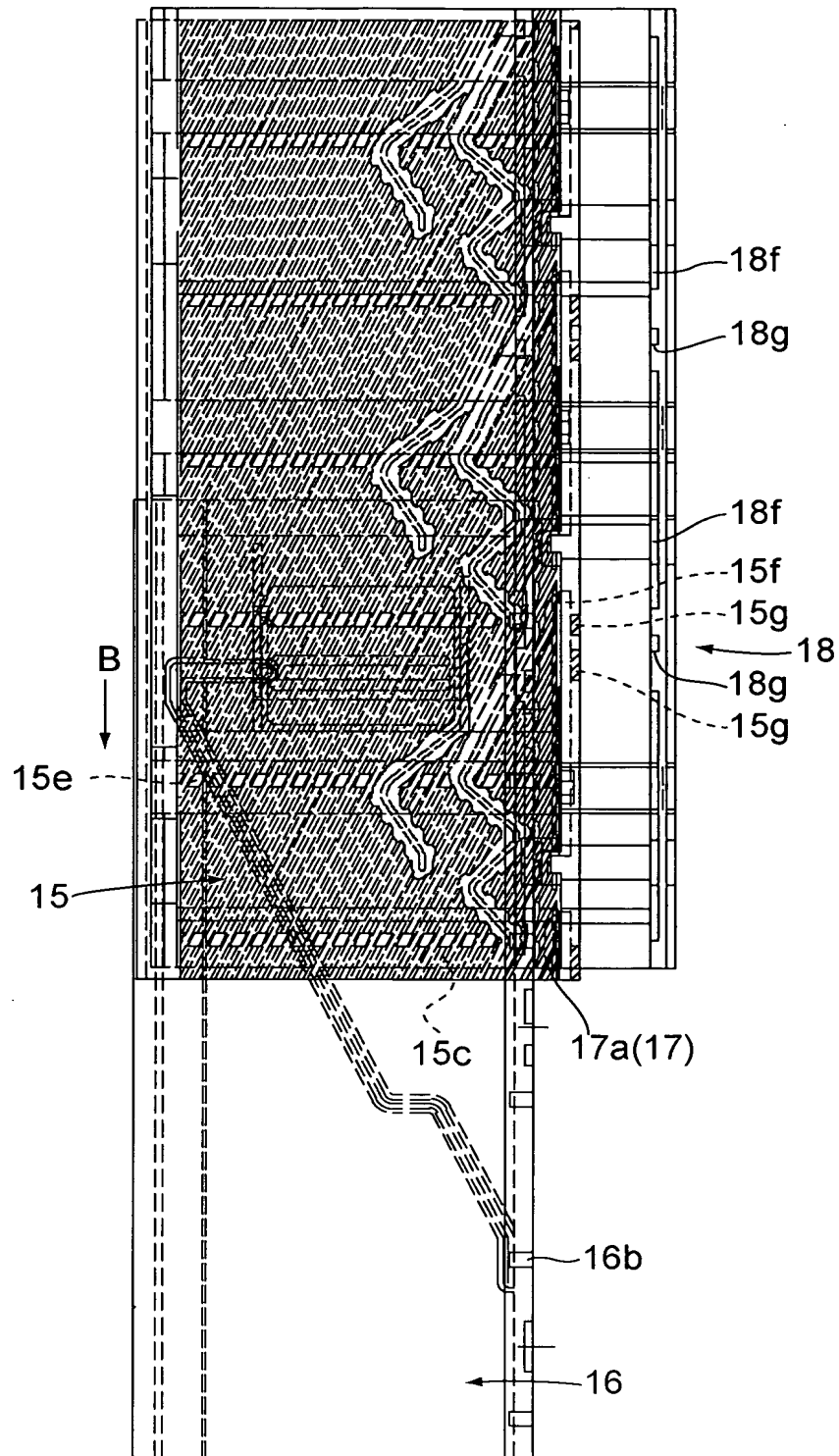


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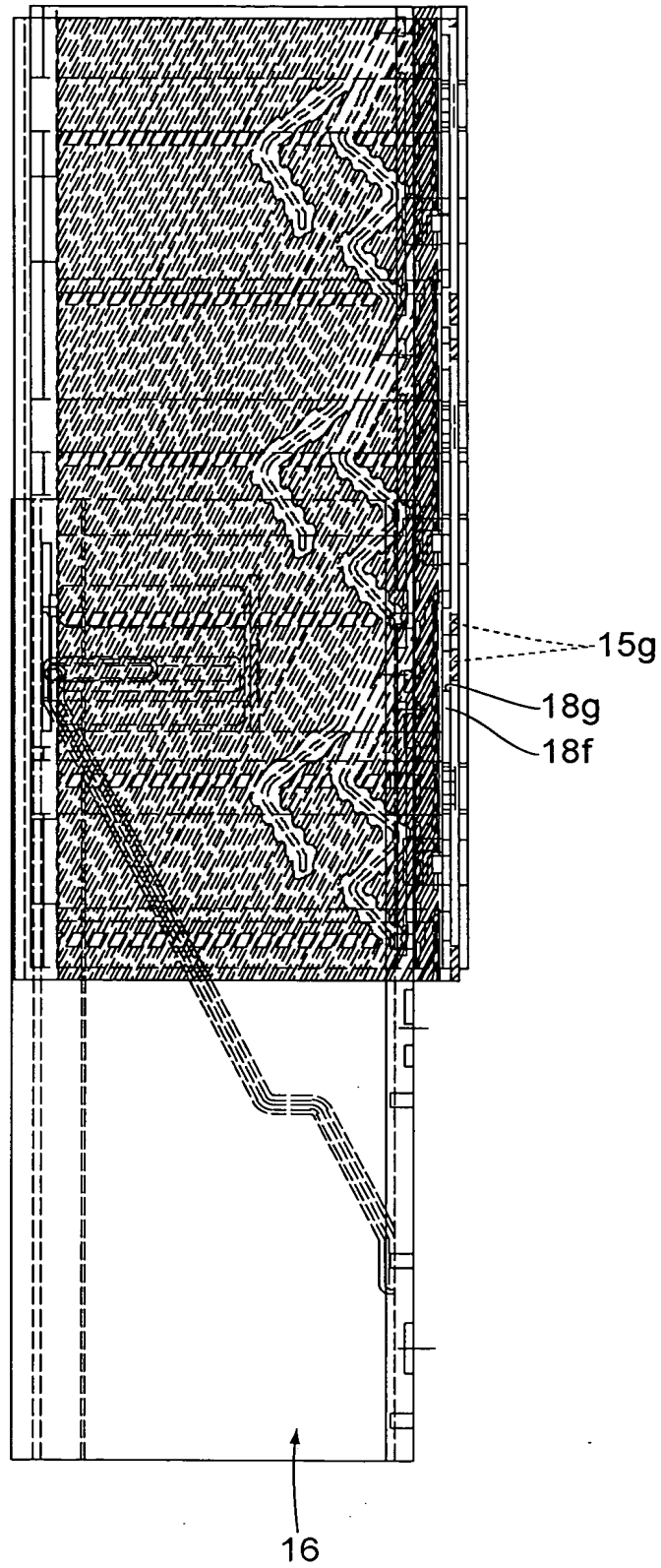


Fig. 44

